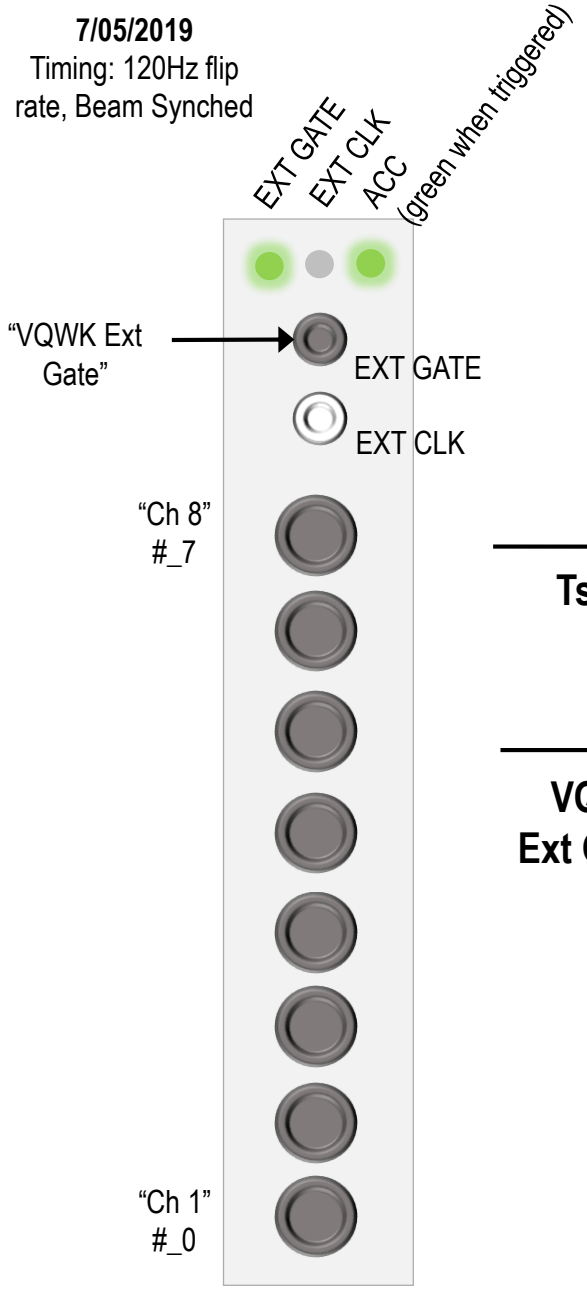
Qweak ADC

7/05/2019
Timing: 120Hz flip rate, Beam Synched



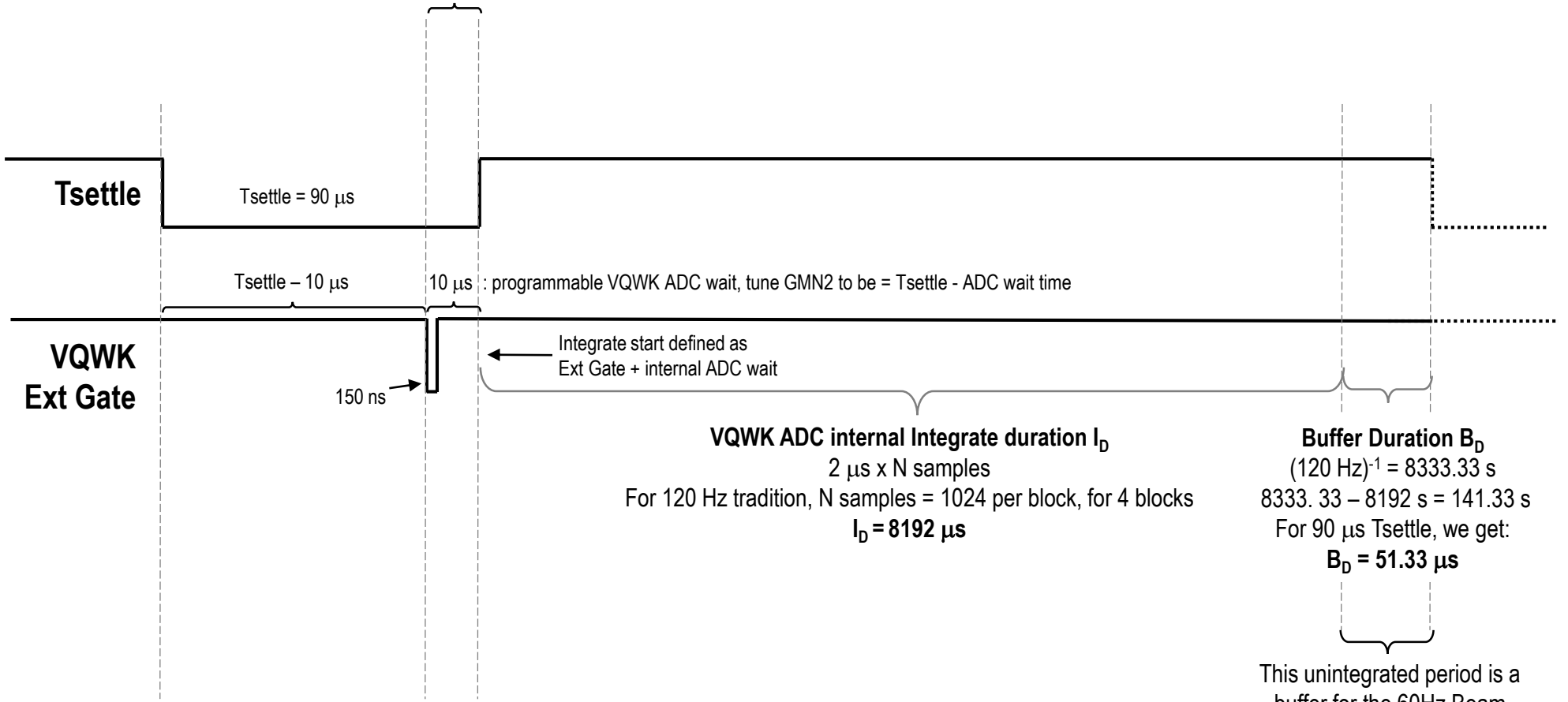
VQWK ADC Timing Notes

- VQWK Ext Gate start defined by Tsettle triggered HAPTB GMN2 G.G. output
- This requires scanning, tuning, and setting default HAPTB ramp delay time to achieve VQWK gate start's 10 us hold-off
- The 10 us hold-off is intended to allow VQWK ADC internal wait time to be > 0 and have its' integration start as close to Tstable as possible

Point to Point in/out map

Input: "VQWK Ext Gate"

- CH: LL NIM Bin Slot 5; Region 3 output 1-6 or Region 4 output 3-4
- INJ:
- RHRS: Betty d7, NIM Bin 726 input #11
- LHRS: Betty a13, NIM Bin 726 input #7



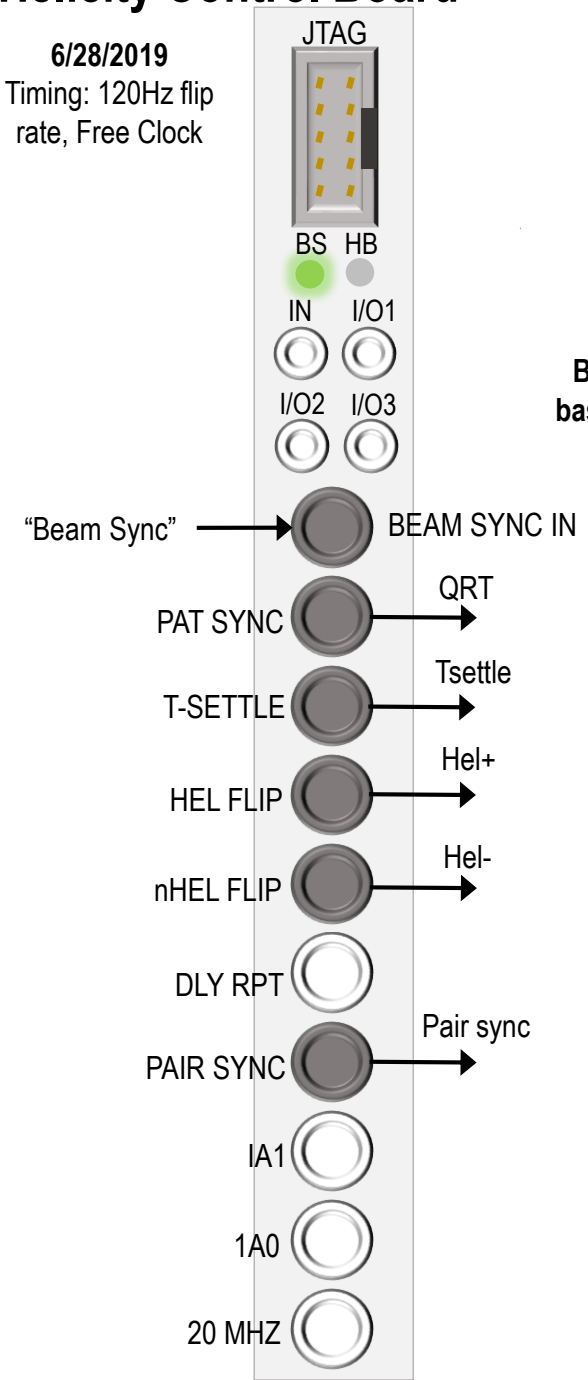
VQWK ADC internal Integrate duration I_D
2 μs x N samples
For 120 Hz tradition, N samples = 1024 per block, for 4 blocks
I_D = 8192 μs

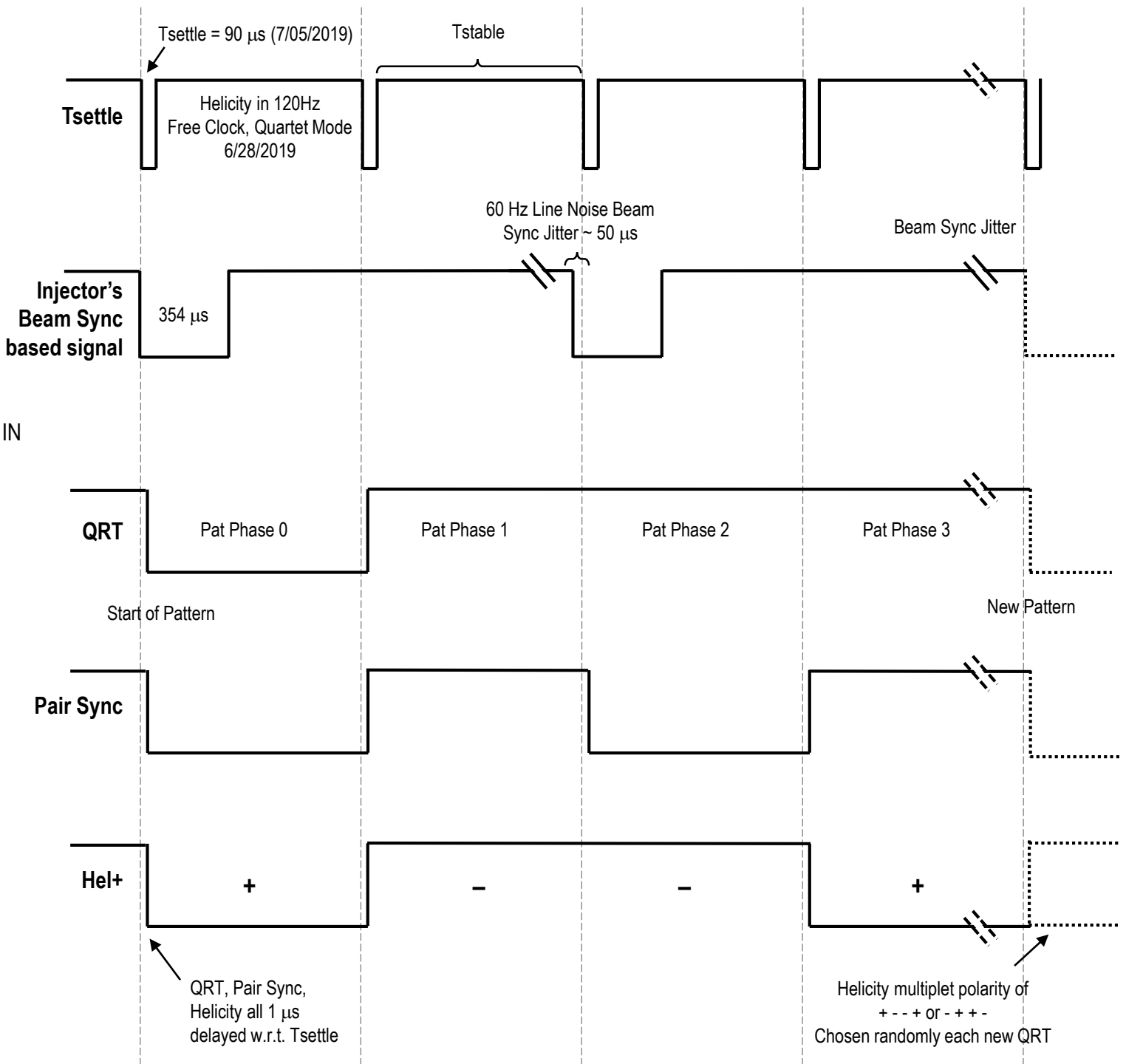
Buffer Duration B_D
$(120\ Hz)^{-1}$ = 8333.33 s
8333. 33 – 8192 s = 141.33 s
For 90 μs Tsettle, we get:
B_D = 51.33 μs

This unintegrated period is a buffer for the 60Hz Beam Sync timing jitter in final multiplet window

Helicity Control Board

6/28/2019
Timing: 120Hz flip rate, Free Clock





P2P in/out map

Input: "Beam Sync"
- INJ: 60 Hz line synced

Output: "Pat Sync"
- CH: Fiber P.P. -> NIM trans 1
- INJ: Fiber P.P. -> VME trans

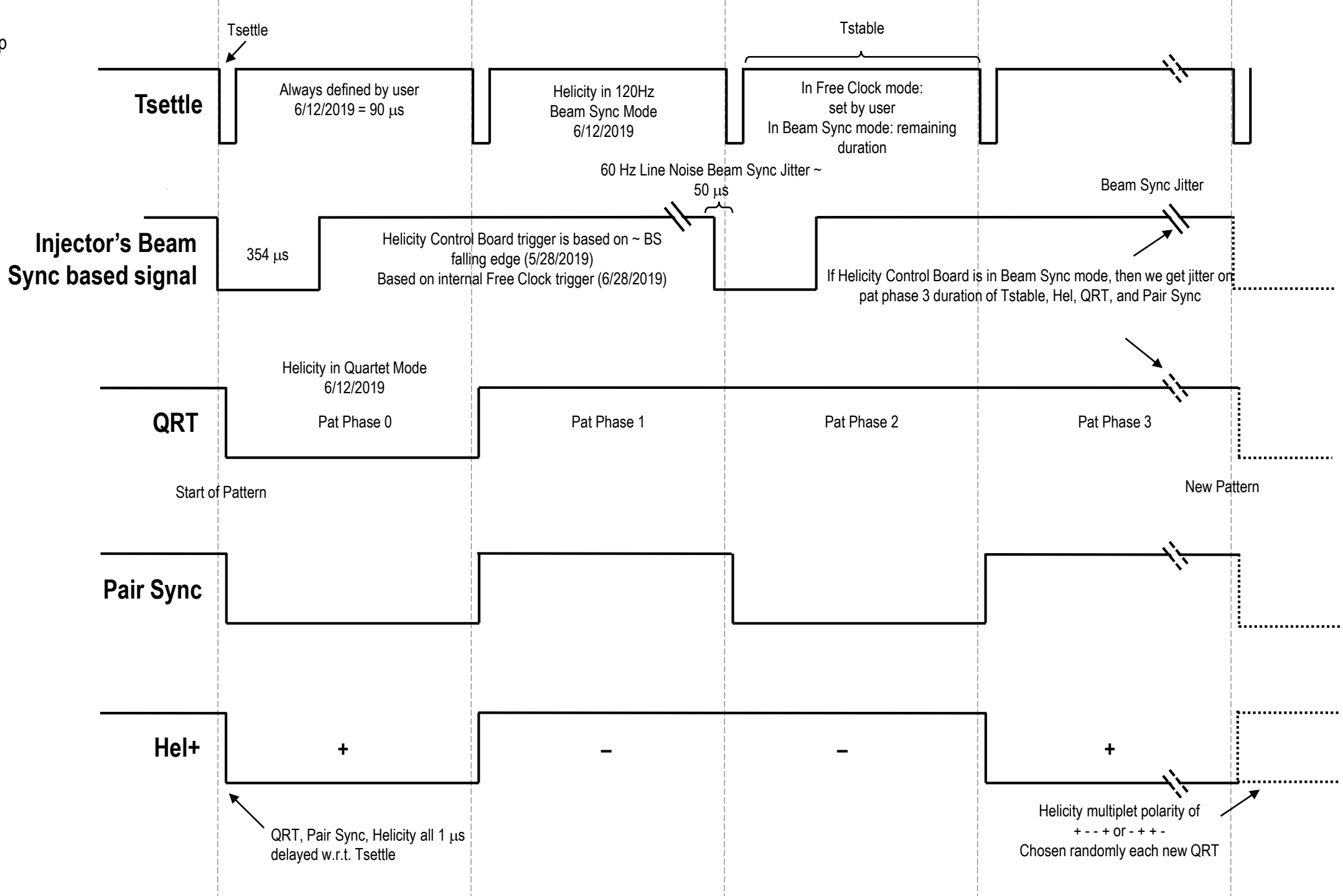
Output: "T-Settle"
- CH: Fiber P.P. -> NIM trans 2
- INJ: Fiber P.P. -> VME trans

Output: "Hel Flip"
- CH: Fiber P.P. -> NIM trans 3
- INJ: Fiber P.P. -> VME trans

Output: "Pair Sync"
- CH: Fiber P.P. -> NIM trans 4
- INJ: Fiber P.P. -> VME trans

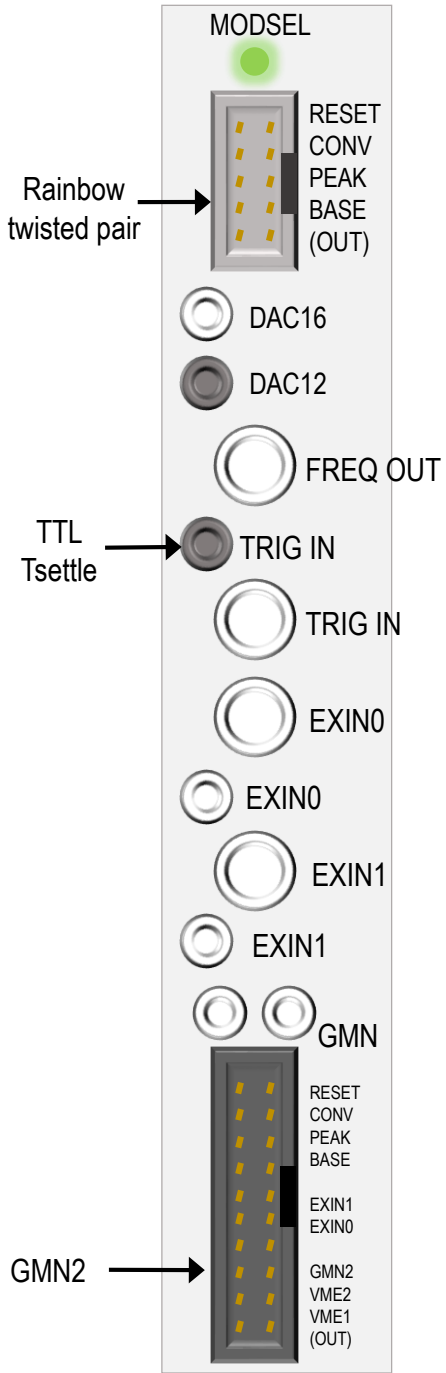
Helicity Information Diagram

6/28/2019
Timing: 120Hz flip rate, Free Clock



HAPPEX TIMER

6/28/2019
Timing: 120Hz flip rate, Free Clock



P2P in

Input: Tsettle

- CH: Lower Left NIM Bin 726 channel 1 TTL
- INJ:
- RHRS: Betty d6 -> NIM Bin 429A -> 726 TTL
- LHRS: Betty a11 -> NIM Bin 429A -> 726 TTL

out map

Output: Rainbow Flat Cable

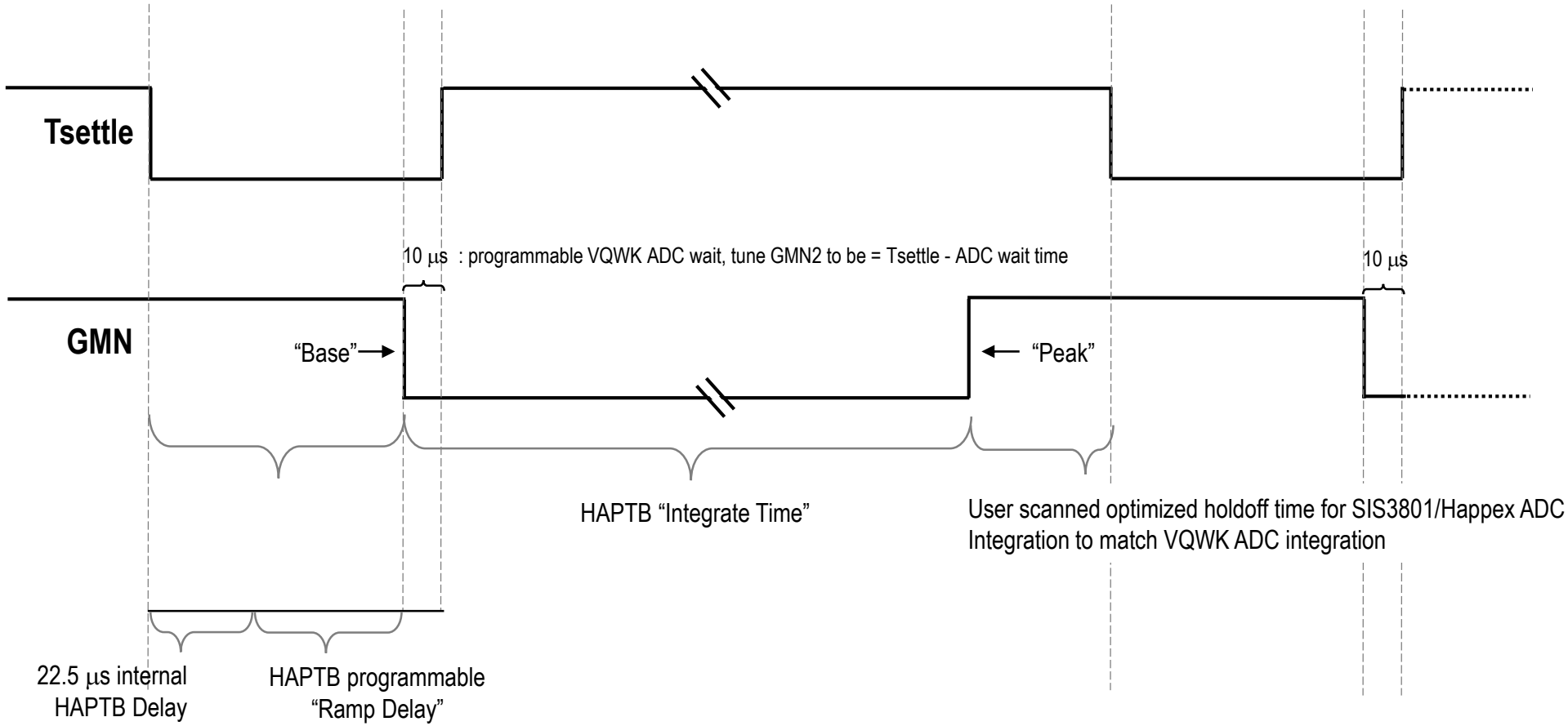
- RHRS: To HAPPEX ADC Chain
- LHRS: To HAPPEX ADC Chain

Output: GMN2 – Twisted Pair dECL

- CH: To SIS3801 VETO and VQWK ADC Ext Gate G.G.s for CH and HRSs
- INJ: To SIS3801 VETO and VQWK ADC Ext Gate G.G.s for INJ

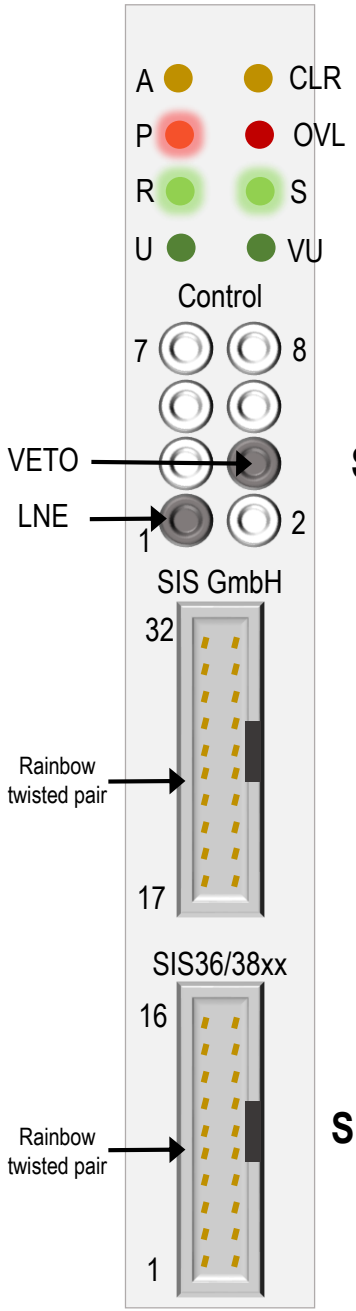
Output: DAC 12

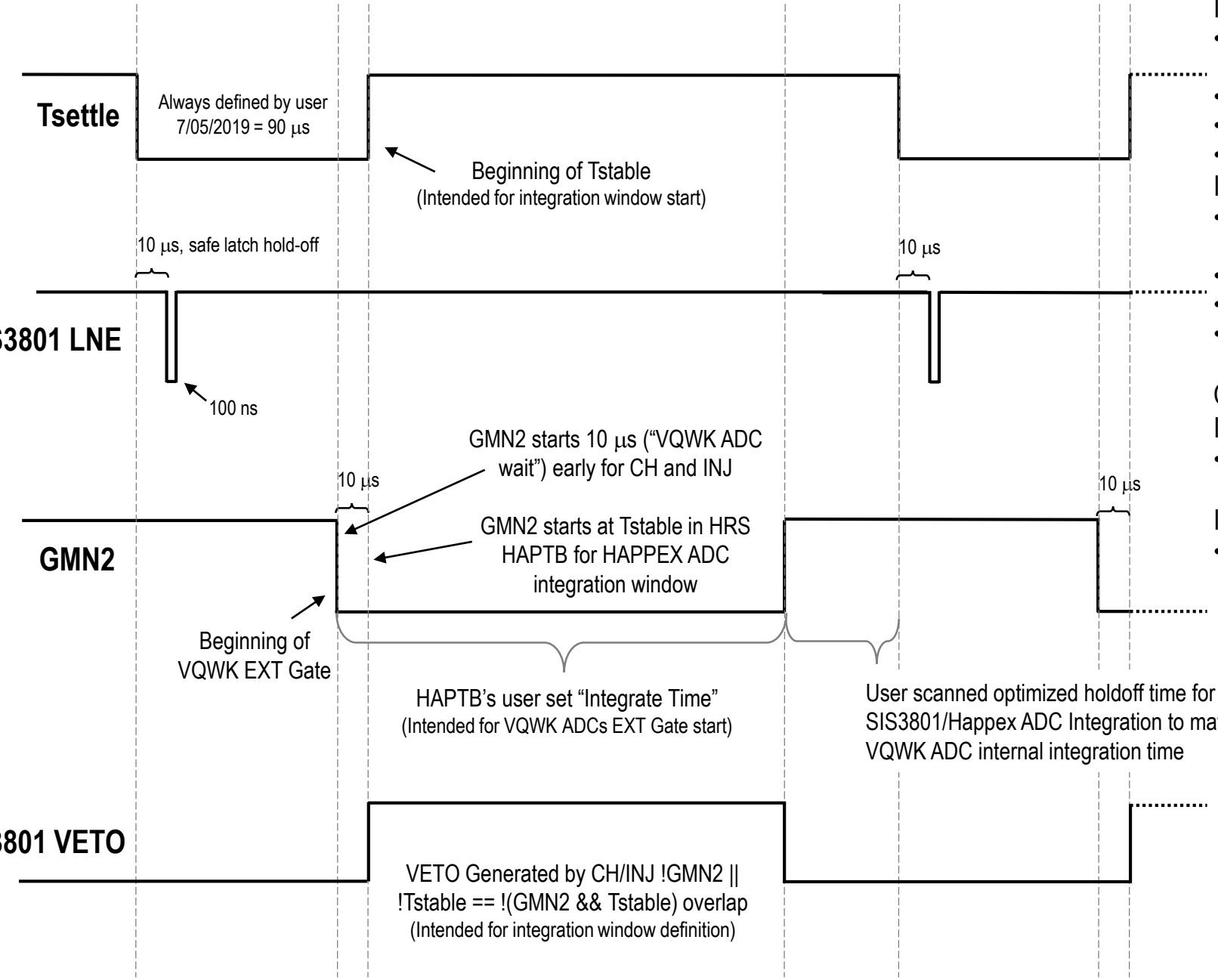
- CH: To synch-frequency generation system (V2F #1, in Ch 16)



SIS3801 SCALER

6/28/2019
Timing: 120Hz flip rate, Free Clock





P2P in/out map

Integrating Scaler

Input (LNE): SIS3801 LNE

- CH VME slot #5: Lower left NIM Bin 429A
  Slot 11, Region 1, Out 3
- INJ:
- RHRS: Betty d2
- LHRS: Betty a10 -> NIM Bin 726 #10

Input (VETO): !GMN2 || !Tstable

- CH vme slot #5: Lower left NIM Bin 429A
  Slot 10, Region 4, Out 3
- INJ:
- RHRS: Betty c8
- LHRS: Betty a14

Clock Timing Scaler

Input (LNE): SIS3801 LNE

- CH #19: Lower left NIM Bin 429A
  Slot 11, Region 1, Out 4

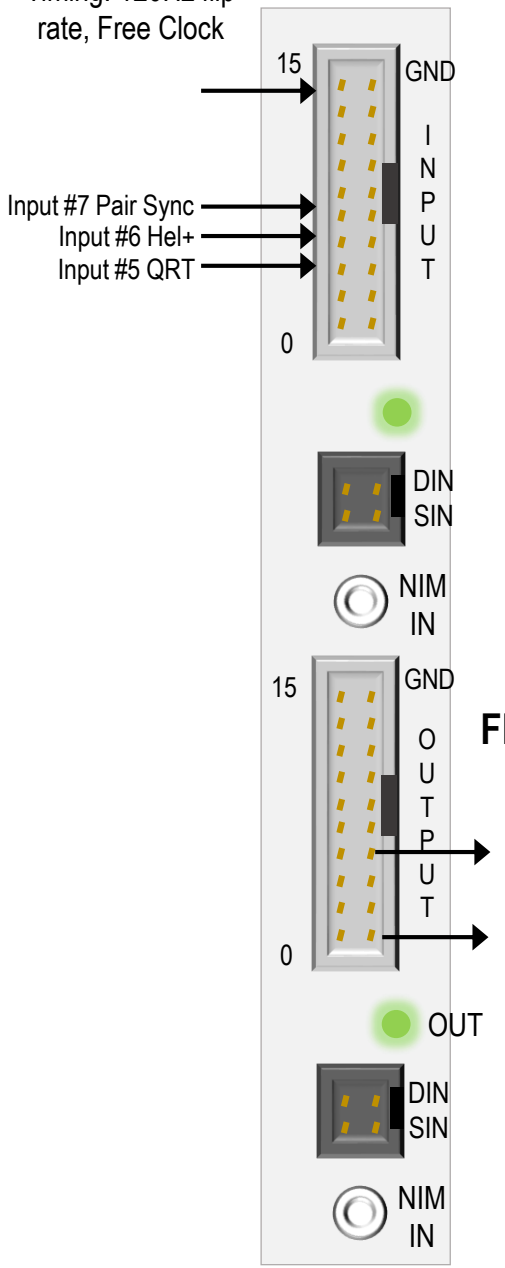
Input (VETO): Tsettle

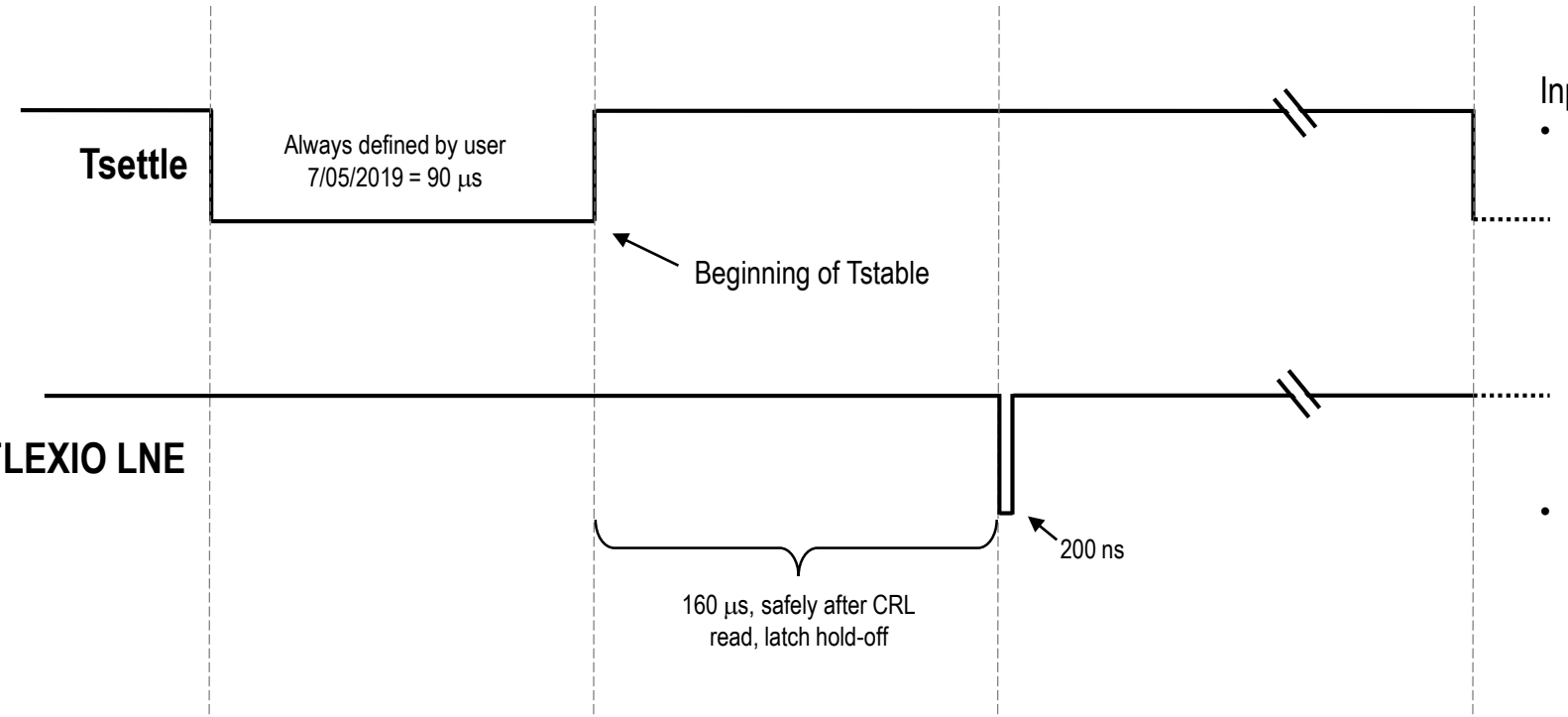
- CH #19: Lower left NIM Bin 757
  Slot 5, Region 3, Out 8

FLEXIO

6/28/2019

Timing: 120Hz flip rate, Free Clock





P2P in/out map

Input (LNE): FLEXIO LNE

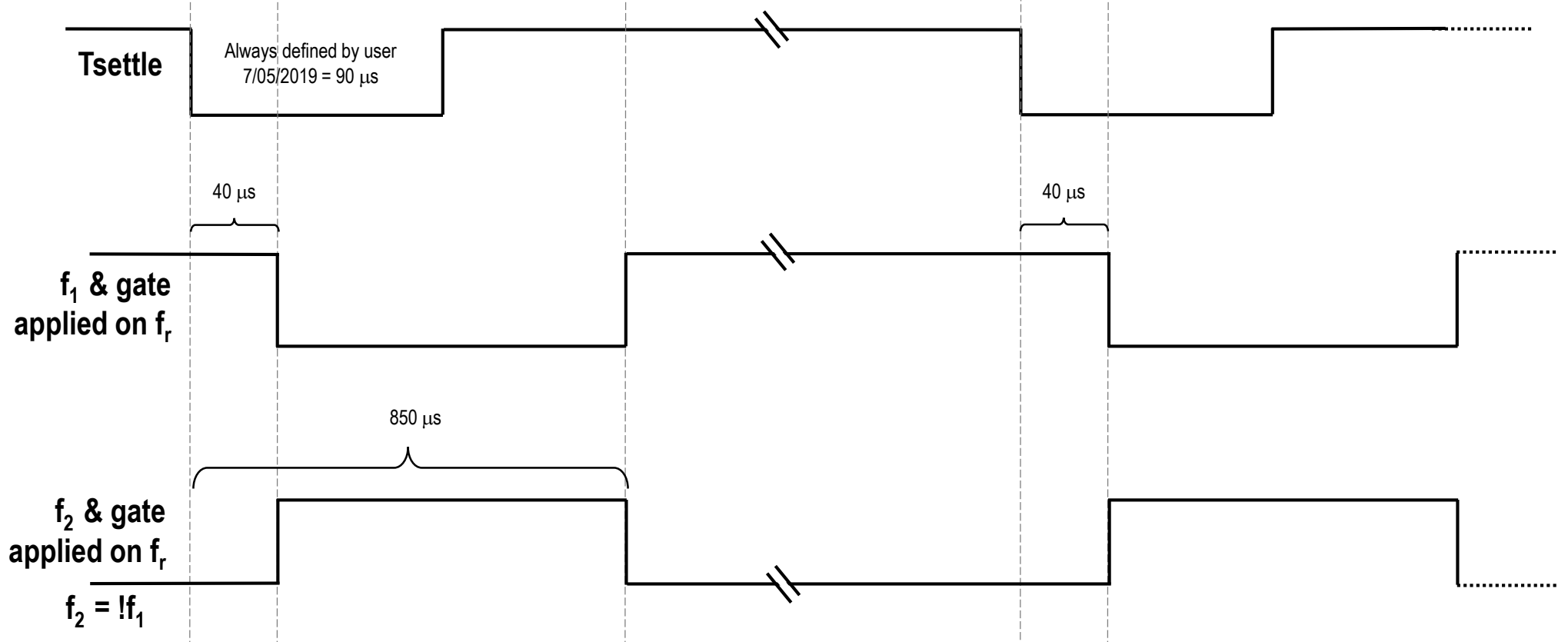
- CH: Lower left NIM Bin 429A
  Slot 11, Region 3, Out 3 -> Lower Left 726 in channel 3 -> red-blue twisted pair to FLEXIO SIN ECL
- INJ:
- RHRS: Betty d5
- LHRS: Betty a12

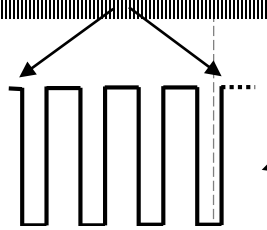
Input (Helicity Info):

- CH
  QRT: pink-grey ECL twisted pair from Fiber Translator 1, out 2, to Input #5 (reversed polarity)
  Hel+: blue-white ECL twisted pair from Fiber Translator 3, out 1, to input #6 (reversed polarity)
  Pair Sync: red-black ECL twisted pair from Fiber Translator 4, out 1, to Input #7
- INJ
  Hel+:
  QRT:
  Pair Sync:

V2F Sync Scaler Check

6/28/2019
Timing: 120Hz flip rate, Free Clock





Spacing between pulses (frequency) determined by CH HAPTB DAC12 voltage, which is a random number set in the CRL for each event ~ 3-7 Volts, plugged into CH 4MHz V2F#1 channel 16

"Constantly true" series of ~125 ns long pulses
Elongated to 200 ns pulses in gates where f_1 and f_2 are applied

These f_1 and f_2 signals are generated in the CH and integrated with the CH/INJ sourced SIS3801 VETO in the integration scalers in CH, INJ, and HRSs