Parity DAQ

Start at 1 for Bits

Start at 1 for NIM Bins & outputs

	CH A								
	Rack	Type	Module, slot, name	Inputs	In Type	Timing Wrt Tsettle	Outputs Destinations	Type	delay
a	CH01 B03	NIM Bin, Helicity Receiver	Helicity Translator 1, leftmost, "QRT"	1) Injector QRT from Fiber Patch panel	Fiber	1 μs after start	1 empty 2 empty 3 empty 4 empty (5) VME scaler FLECCO input ch 5 6 empty (7) LeCroy 429A CH01B03 slot 6 input ch 4 8 empty 9 empty	Fiber Fiber Fiber ecl ecl ecl LEMO LEMO LEMO	2n
b	"	"	Hel trans, 2, "MPS"	1) Inj MPS from Fiber PP	Fiber	$== \overline{T_{settle}} = T_{stable}$	1-6 empty (7) LeCroy 429A CH01B03 slot 6 input ch A 8 Broken 9 Broken	(fiber x3, ecl x. LEMO LEMO	2u
c	"	"	Hel trans, 3, "HEL"	1) Inj Hel+ from Fiber PP	Fiber	1 μs after Start	1-6 empty * (7) Moller Hel+ (8) 726 lvl trans CH01B03 slot 7 input ch 13 * (9) Moller $\overline{Hel+}$? → 9 + 10 = out "3rd Hel" CH01B04 bottom patch Panel input # 7 input # 14 (10) New Compton NIM out	) fiber x3, ecl x3 LEMO LEMO	6u 2us 6 us
d	"	"	Pair Sync, 4, "PairSync"	1) Inj Pair Sync from Fiber PP	fiber	1 μs after Start	1-5 empty ← (6) 726 lvl trans CH01B03 slot 7 ecl input ch 5 * (7) Somewhere downstairs "HAPPEX" (8) 726 lvl trans CH01B03 slot 7 input ch 3 (9) Patch Panel "BOOR h1H75TB03" Channel 11, CH01B04 (10) CH01B06 slot 2 FERO	fiber x3, ECL x2 ecl LEMO LEMO LEMO → BNC w 6. LEMO	5 ns ? 2 ns Tpo

NEW Bypassed lvl trans, got straight from Fiber trans

has really bad noise in 726 outputs

To do: replace HRS

These signals should be streamlined through a set of FIFO's & the Hel+ information should be minimized & not touch any Neighboring NIM Modules if possible

Parity DAQ

CHA

Rack #	Type	Module, Slot, Name	Inputs	In Type	Timing WRT Tsettle	Outputs Destinations	out Type	out cable delay	notes
CH01B03	NIM Bin, Helicity Receiver	Lecroy 429A FiFo, 6, Logic FIFO	1) set of 4 inputs tied together empty, Tape over it	LEMO	~~empty~~	empty	LEMO		
"	"	"	2) Set of 4 inputs only one used, Tstable from Ⓑ	LEMO	= = $\overline{Tsettle}$ = Tstable	out $\overline{out}$ out ● ○ ○ ○ ○ ○ → 726 lvl trans CH01B03 slot 7 input ch 7	LEMO	1 ns	
"	"	"	"			○ ○ ○ ● ○ ○ → "3rd MPS" signal ch5 to PP "50Ω to 1H75B03 in HALL A"	LEMO	~ 5 ns	I took a sketchy cable connection out + shortened length from 10 ns to 5...
1	"	"	"		output = $\overline{in}$ = Tsettle	○ ● ○ ○ ○ ○ → 726 lvl trans CH01B03 slot 7 input ch 1	LEMO	~ 2 ns	== Tsettle
4	"	"	"		output = $\overline{in}$ = Tsettle	○ ○ ○ ○ ● ○ → "MOLLER MPS" sig ch16 in PP "50Ω to 1H75B03 in Hall A"	LEMO	~ 10 ns	== Tsettle
5	"	"	"			○ ○ ● ○ ○ ○ → CH01B06 slot 4 Quad Linear fifo Input ch 1	LEMO	~ too long	too long, unknown function... Wasted Fifo?
6	"	"	"			○ ○ ○ ○ ○ ● → empty	LEMO		
12	"	"	3) Set of 4 inputs only one used, from 429A FiFo, CH01B03 slot 12, out 3 out ch ○ ○ ● = GMN2	LEMO	120 ns after Tsettle falling edge, = VQWK start integrate "EXT gate" for now	out $\overline{out}$ out ● ○ ○ ● ○ ○ → Both go to VQWK EXT Gate directly	LEMO	~ 10 ns	Can be optimized in + output
2	↑ improvable →					○ ○ ● ○ ○ ○ → CH01B05 PP "to left arm detector stack" ch 7, sends VQWK ext gate	LEMO	~ 15 ns	
5	"	"	"			○ ○ ○ ○ ○ ● → CH01B06 PP "to right arm detector stack ch 8, feeds VQWK ext gate	LEMO	~ 15 ns	
6	"	"	"			○ ● ○ ○ ● ○ → Both empty	LEMO		
3 + 4	"	"	"						
H1 H4	→ else empty		4) QRT from @ ch 7	LEMO	1 μs after tsettle	empty other wire ○ ○ ○ ● ○ ○ → CH01B06 slot 4 Quad Linear fifo input ch 2	LEMO	too long	Wasted fifo? Physically

Parity DAQ

CHA

0	Rack #	Type	Module, Slot, Name	Inputs	In type	Timing wrt Tsettle	outputs Destinations	Type out	out cable delay	notes	
.	CH01B03	NIM Bin, Helicity Reciever	726 level translator, 7, "The monster"	1-3, 6-8, 10-16 + gnd	empty ECL						
4e+l	"	"	"	4) VME TI board out 7	ecl	?	empty	ecl + LEMO		empty!	
5e+l	"	"	"	5) Pair sync, ⓓ ch 6	ecl	1 μs after	empty	ecl + LEMO		empty!	
9 lemo	"	"	"	9) GMN2, from HAPTB	ecl	120 μs after	same module ch 10..... eventually fans out to all vqwks	LEMO, (ecl empty)	complex	source of GMN needs improvement	
1 ecl	"	"	"	1) Tsettle from ⓕ3	LEMO	== Tsettle	out LEMO 1 → CH01B03 429A slot 11, input section 2, only input	LEMO	3 NS		
							" out LEMO 2 → CH01B02 upper NIM Bin slot 7, 794 gate generator, in section 3 trigger	LEMO	8 NS	Sych Monitor MPS source	
							out ECL → VME scaler SIS3801 input "15" (index = 14)	ECL	~ 4 NS	scaler readout	
i2 ecl	"	"	"	2) Helt from CH01B03 slot 11 429A 4th set of FIFO			VME Flex IO input 7	ECL	~ 4 NS	could be used probably worse source !	
i3 lemo	"	"	"	3) Pair sync from ⓓ ch 8	LEMO	1 μs After →	long single out put lemo to unknown destination	lemo			
i3 ecl	"	"	"	3) "	"	"	VME flex IO input 8	ecl	~ 4 NS	needed?	
i6 ecl	"	"	"	6) Unknown source, some V2F	LEMO	V2F signal	ecl to VME SIS3801 scaler input ch 11 (index 10)	ecl	~ 4 NS	move it what is it?	
i7 lemo TTL	"	"	"	7) Tstable from ⓕ4 lemo →	LEMO	== Tstable MPS	TTL out put → Haptb trig in	LEMO	8 ns	MPS or MPS needed?	
i7 lemo NIM	"	"	"	7) "	"	"	2nd NIM output → 429A slot 11 in set 2, in ch 1, to fan out	LEMO	1 us	needs help !	
i8 ecl	"	"	"	8) 13.5 kHz pulser Pulser	LEMO	random	VME SIS3801 scaler 2n ch 14 (index 13)	ecl	4 ns	for speed / deadtime testing	
i10 lemo	"	"	"	10) GMN2 from ⓕ9 lemo	LEMO from ⓕ9 lemo	120 μs after	to 429A slot 11 in set 3, in ch 1, to fan out to all vqwks ext gate	LEMO	1 us	needs help	
i13 lemo TTL	"	"	"	13) Helt from ⓒ8	LEMO	1 μs after	one goes to Compton via TTL out fiber converted to	LEMO	long	Compton	
i13 lemo NIM	"	"	"	13) "	lemo	1 ms after	NIM goes to 429A slot 11 in set 4, in ch 1	LEMO	1 us		
16 lemo											

Parity DAQ

CH A

	Rack #	type	Module, Slot, Name	Inputs	In type	Timing wrt Tsettle	outputs destinations	Type out	out cable delay	notes
0	CH05B03	Nim Bin, Helicity receiver	Lecroy 222, 8, dual gate generator	Its 2 gate generators that feed on themselves → no connection to external cables.....						
-	"	"	"FR AC Switch", 9	unlabelled cable	BNC	?	→ It has a note taped "don't unplug or turn off, will shut off the beam)			
(	"	"		→ just an unused module....						
[	"	"	"MPS Missing"							
1	"	"	Lecroy 429A, 11 logic fifo	1) i27 Lemo Nim Tstable from f1	lemo	== Tstable	out out out ● ○ ○ / ○ ○ ○ → Ch 18 "mps to comptom" in TP of CH01B04	LEMO	~10 ns	can be optimized
3	"	"	"	1) "	"	"	○ ● ○ / ○ ○ ○ → in set 1 only input of slot 1, model 622, CH01B02 upper NIM	LEMO	~6 ns	Tsettle for Beam mod?
6	"	"	"	1) "	"	"	○ ○ ○ / ○ ○ ● → off to CH03B02 upper NIM slot 4, 110 quad FIFO	LEMO	6 ns	Tstable, sent down below wasted Quad FIFO
s_1	"	"	"	2) i1 Lemo from f3	lemo	== Tsettle	● ○ ○ / ○ ○ ○ → VME SIS3801 control in 1 LIVE	LEMO	8 ns	Tsettle LIVE?
k_2	"	"	"	2) "	"	"	○ ○ ○ / ● ○ ○ → "To Right Arm Detector stack" Patch panel Ch 2	LEMO	~15 ns	"
k_5	"	"	"	2) "	"	"	● ● ○ / ○ ○ ○ → VME SIS3801 control in Ch 4 veto	LEMO	8 ns	Tsettle veto?
k_6	"	"	"	2) "	"	"	○ ○ ○ / ○ ○ ● → "To left arm Detector stack" Patch Panel ch 10	LEMO	~10 ns	Tsettle LIVE?
l_1	"	"	"	3) GMN2 from i10 lemo	"	= 120 ns after	● ○ ○ / ○ ○ ○ → to vqwk ext gate	LEMO	~10 ns	GMN2 gate?
l_2	"	"	"	3) "	"	"	○ ○ ○ / ● ○ ○ → "	LEMO	~6 ns	GMN2 gate?
l_5	"	"	"	3) "	"	"	○ ○ ● / ○ ○ ○ → "	LEMO	~6 ns	"
l_6	"	"	"	3) "	"	"	○ ○ ○ / ○ ○ ● → (9) input fifo again	LEMO	6 ns	"
m_1	"	"	"	4) i13 Lemo NIM Helt	"	1 ns after	● ○ ○ / ○ ○ ○ → (i2) input	LEMO	3 ns	Helt noise some?
m_6	"	"	"	4) "	"	"	○ ○ ○ / ○ ○ X → goes down to beneath?	LEMO	?	?
n	"	"	Dual adc	1) To [illegible]		To [illegible]	"Gate"			

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Parity DAQ
Ch A

	Rack #	type	Module, Slot, Name	Inputs	In Type	Timing wrt Tsettle	Output destinations	Type out	out cable delay	notes
1	CH01B02	NIM Bin upper	Lecroy 622 quad coinc, 1	1) "Or" mode, in 1 only = Tsettle (O3)	LEMO	== Tsettle	Tsettle → NIM bin upper slot 8 input ch 1	lemo	~8ns	why?
2										
3	"	"	"	1) "	"	"	Tsettle → same module in slot 4	lemo	1ns	why?
5	"	"	"	1) "	"	"	Tsettle → ~~removed.~~			
7	"	"	"	2) "or" mode, in 1 only = synch test f_2 signal gated/strobed	LEMO	V2F signal	→ to upper NIM bin slot 6 ch 2 output NIM	lemo	3ns	send thru a NIM→Fiber
2	"	"	"	2) "	"	"	→ to LHRS pp ch 11	lemo	12ns	
4	"	"	"	2) "	"	"	→ to upper NIM bin slot 2 726 Lvl trans input 3	lemo	1ns	f_2? or ~~f_1~~
6	"	"	"	2) "	"	"	→ to RHRS pp ch 5	lemo	~15ns	~~f_1~~
1	"	"	"	3) f_2 signal gate strobed	"	"	→ to upper NIM bin slot 6 ch 2 output NIM	lemo	3ns	needs NIM→Fiber trans.
2	"	"	"	3) "	"	"	→ To LHRS pp ch 12	lemo	12ns	f_2 or ~~f_1~~
5	"	"	"	3) "	"	"	→ to upper NIM bin slot 2 726 Lvl trans input 2	lemo	2ns	"
6	"	"	"	3) "	"	"	→ to RHRS pp ch 12	lemo	~15ns+	"
3	"	"	"	4) "And" of undelayed signal + (O3) tsettle	LEMO	"	→ upper NIM bin slot 7, 794 gate generator in set 1, input trigger	lemo	~4ns	what is it?
9-16	"	"	726 Lvl trans, 2	9-16) From slot 11 V2F beammod signals	ECL	?	Twisted pair → flat cable sends to chs 12-32 of SIS3801 UME inputs	flat cable	~6ns	BMod... could be improved
15	→ 4MHz reference			BMod #2-9+16) = 4MHz ref slot 10						
1, 1	ecl lemo	"	"	1) "Sync f_2" from slot 8 "out8"	lemo	Haptb ramp dw 12, V2F	NIM out 1 → slot 3 756 quad logic input ch 1	lemo	1ns	f_2 source
1, 2	ecl lemo	"	"	1) "	lemo ledlo	"	NIM out 2 → slot 3 756 quad logic input ch 2	lemo	1ns	f_1 source
2	ecl	"	"	2) "Sync f_1" from (Q5)	ledlo	Sync check f_2	ecl out → scaler ch 17 (index 16) for sync f_2 reference	Flat cable	~6ns	f_2 signal for sync monitor
3	ecl	"	"	3) "Sync f_2" from (P4)	lemo	Sync check f_2	Scaler input ch 18 (index 17)	Flat cable	~6ns	to scaler
4	TTL	"	"	4) "BMW Trig BMW"	lemo	?	Scaler input ch 19 (index 18)	Flat cable	~6ns	
							TTL → BMW Busy "#1"			

b

Parity DAQ

CHA	Rack#	Type	Module, Slot, Name	Inputs	In type	Timing wrt Tsettle	output Destinations	Type out	out cable delay	Notes
T_1	ch01002	NIM Bin Upper	756 quad logic unit, 3	1) a) "fr" ($S_{1,1}$)	lemo	Hapt6 rampdac 12	(P_2 in), after veto	lemo	1 ns	(comes fr
T_{2veto}	"	"	"	1) veto) gate of slot 7, 794 out set 2	lemo	58 μs after Tsettle	↗	~~lemo~~		
T_{2a}	"	"	"	2) a) "fr" ($S_{1,2}$)	lemo	Hapt6 rampdac 12	(Q_1 in), after veto	lemo	1 ns	(comes fr
				2) veto) gate of slot 7, 794 out set 2	lemo	1.75 ms after Tsettle	↗	~~lemo~~		
T_{2veto}	"	"	"							
$T_{3,1}$	"	"	"	3) a) "BMW MPS" "delay" out of 794 outset 2	lemo	?	(S_4 in)	lemo	2 ns	?
$T_{3,2}$	"	"	"	3) b) "BMW Flexio gate" "gate" out of 794 outset 4	~~lemo~~ lemo	?	"BMW gate reset" to 794 inset 4 "reset"	lemo	2 ns	?

Crime level 2

T_4 empty

U_1	"	"	740 quad lin FIFO, 4	gate output of 794 outset 4	lemo	?	dead end			
U_2	"	"	"	(16 output → Tstable from F_1)	lemo	≐ Tstable	goes down to depth 5	lemo	?	
U_3	"	"	empty							
V	"	"	homemade fiber→NIM trans, 6	has f_1 + f_2 from P_1 Q_1	lemo	V2F synch test	sends to 60 transceiver rack; needs to be NIM→fiber trans	Want Fiber	?	need module
W_1	"	"	794 quad gategenerator, 7	1) Trig in) (K_3 Tsettle + ?)	lemo	1 μs after Tsettle, 600 ns long	Gate signal is the "delayed" option for coupler MPS	lemo	long	destruct? redo better?
				1) delay) weird VME module	lemo	? empty signal?	same "	〃	〃	〃
W_2	"	"	"	2) Trig in) (W_3 gate output)	lemo	~60 μs after	Gate → f_2 veto	lemo	~3 ns	f_2 veto
				2) delay) ($T_{3,1}$ input a)	lemo	?	Gate → f_1 veto (starts 60 μs after tsettle, lasts ~2.3 ms (= 1/2 240 Hz))	lemo	~3 ns	f_1 veto
W_3	"	"	"	3) Trig in) Tsettle (i_2 out lemo 2)	lemo	== Tsettle	(W_2 trig in) gate output	lemo	1 ns	(source of gate
W_4	"	"	"	4) Trig in) Tsettle (X_1 out)	lemo	?	gate → ($T_{3,2}$ b)	lemo	~~1 ns~~ 3 ns	BMW
				4) reset) ($T_{3,2}$)	lemo	?	~~gate → dead end (U_1)~~			
X_1 NIM	"	"	homemade nim-ecl trans, 8	1) NIM Tsettle (O_2)	lemo	== Tsettle	"BMW flexio" (W_4 trig in)	lemo	2.5 ns	BMW
X_{1ecl}	"	"	"	1) ECL Flexio out "1"	ECL	?	↗	ecl lemo		why Flexio out?
				1) "	"	"	T5 "T1"	ecl	"	why T5 gets?
X_2 Nim	"	"	"	2) " or Rampdac 12	"	Rampdac 12	↗			

Parity DAQ
CHA

ID	Rack #	Type	Module, Slot, Name	Inputs	In type	Timing wrt tsettle	output destinations	Type out	out cable labeling	notes
Y_a	CH01B02	NIM Bin lower	4616 NIM-ECL Trans, 5	1, 2, 3, 4 unknown from slot 10 G23B discriminator	lemo	?	VME S1588 ch 2, 7, 8 respectively	ecl	~10 ns	?????
Y_b	"	"	623B octal discrim 10	2, 3, 4, 5, 6, unknown from below	lemo	?	to Y_a	lemo	?	????
E_1	Rack CH01B06	NIM Bin far left	759 FIFO, 2	D10 PairSync	lemo long	1 µs after	out 1 → to RHRS PP ch 7 out 2 → to LHRS PP ch 9	lemo	5 ns 6 ns	why...?
E_2	"	"	740 Quad FIFO, 4	f_5 in 1 Tstable From ⓑ in 2	lemo long	==Tstable	out 1 → to LHRS PP ch 6 out 2 → to RHRS → dead end	lemo	long	not in use? LHRS only
E_3	"	"	"	f_1 Qrt from ⓐ	lemo	1 µs after	out 1 → TO RHRS PP ch 1 out 2 → TO LHRS PP ch 5	lemo	long	not in use?
IME_1^{TI}	CH01B03	VME	TI Board, 2	"In 0", Haptb "VME1out"	ecl	190 µs before Tsettle ? CRL?	TI Board logic?			
IME_2^{TI}	"	"	"	"Out 0", TI Board logic?	ecl	50 µs after coda Running only, 125 µs long	SIS3801 in #18 (index 17)	ecl	~8 ns	Trig in, stand alone mode
IME_3^{TI}	"	"	"	"out 6", TI Board logic?	ecl	inside CRL	ecl in 7 of X_7 ecl CH01B02 slot 8 upper	ecl	~12 ns	BMW, not in use
IME_4^{TI}	"	"	"	"out 7", TI Board logic	ecl	12 µs after, lasts	ecl in 4 of CH01B03 slot 7 bot	ecl	~8 ns	dead end, not in use
VME_1^{TB}	"	"	Haptb, 3	"out VME1", Haptb logic	ecl	VME_1^{TI} "VME1out" until 50 µs before end	VME_4^{TI} "VME1out" trans	ecl	~8 ns	Trig in TI stand alone mode
VME_2^{TB}	"	"	Haptb "	" Haptb logic	ecl	520 µs after Tsettle after LIVE=Tstable	"BMW2" to all ADC coin gates	ecl	~6 ns	ADC coin gate
VME_1^{SIS}	"	"	SIS3801, 4	Control in 1, LIVE = Tsettle (t_5)	lemo	=Tsettle	logic			
VME_2^{SIS}	"	"	"	Control in 4, Veto = Tsettle (t_5)	lemo	==Tsettle	logic			
$IME^{SIS\,in\,2,7,8}$	"	"	"	Y_a unknown BCMs?	ecl	?				
$VME^{SIS\,in\,11}$	"	"	"	iEcal unknown VZF	ecl	?				
$VME^{SIS\,in\,14}$	"	"	"	iRecl Rocket Relay "clock"	ecl	random				
$VME^{SIS\,in\,15}$	"	"	"	iSecl Tsettle	ecl	==Tsettle				
$VME^{SIS\,in\,16}$	"	"	"	VME_2^{TI} coda Running signal	ecl	VME_2^{TI}				
$VME^{SIS\,in\,17-32}$	"	"	"	BMW scalers & Hodo about it	ecl flat cable	BMW	Data			
VME^{Flecio}										can improve ecl

needed, can improve timing!
Can improve?
?
?
Testing for skipped events + deadtime calc → Can improve

8

BPM 8xm is missing
- I found its cable near 12 xm intended spot
- Test send V2F "fo" through 8xm signal cable
  - ↳ Caryn found it in 35Y by adding 50Ω terminators + checking with multimeter
    - ↳ It was actually BPM 12 the whole time

Compton Patch Panel

Compton Destination	Upstairs PP source	Signal	Type
1	1	PMT	Signal to read
2	18	Hel	3.2 volts TTL out of 1x T26 Rul trans "Hel"
4	19	MPS	1.6 volts "NIM" out of 429A → 726 → 429A "Tstable"
5	17	BCM	V2F out from BCM
3	2	Empty	—

1

New plan, use efficient logic fifo's to send copies of Tstable, Tsettle, Vqwk gate, Scaler LNE, FLEXIO LNE, + hel info around

New Signals

- Narrow Gate for Vqwk gate at Tstable start → x6 for CH ADCs + x2 for HRS pp's → New 794 gate gen3, 10μs long at Tstable "gate"
- Narrow Gate during Tsettle for SIS3801 latch → 2x for potential double in CH + x2 for HRS p.p.s → New 794 gate gen3, 100ns at 10μs "delay" after Tsettle
- Narrow Gate after Tstable + after FLEXIO internal read for FLEXIO Latch → x1 for CH FLEXIO + x1 for BMW read + x2 for HRS pp's → New 794 gate gen3, 150μs later than Tstable + 200ns long "delay"

Accounting what is currently needed and needs replicating

- Hel+: Moller Hel+ p.p., Moller "3rd" Hel+ P.P., Compton TTL (→ swapped for NIM) Hel+, unknown basement Hel+, ECL FLEXIO Hel+ in CH (avoid scaling to the HRSs)
  - ↳ These all fit in the fiber translators outputs now

10/4/2019 → Decabled Hel+ in NIM Bin + all come from fiber translator spigot now → Took care to keep same polarity in all signals, including ECL cable, though it will need verification later

- PairSync: Unknown Downstairs, P.P. "50Ω to IH751303", Flexio ECL, "Hopper" downstairs, (2x defunct HRS p.p.) (turn into LNEs)
- QRT: One copy needed for Moller polarimeter (currently testing QRT), other copy is 2x defunct HRS p.p.s which should turn into DAQ LNE's
- MPS: I moved all Tstable + Tsettle to New 757 logic FIFO
- Vqwk Gate: I made a 10μs long == Tstable gate and put it into bottom half of 757 FIFO

Unplugged Hel's + FLEXIO got polarity swapped, so debugging

/- Run 1588 - Doesn't decode correctly → works

:- Run 1589 - Re wire hel (flipped) → fail

:- Run 1590 - Re wire hel + QRT → fail
(unflip, flip) (it is inverted at fiber source....)

- Run 1591 - unflip QRT, push 3 signals 1 input channel higher → definitely wrong

/- Run 1592 - flip pairsync, nope → works

/- Run 1593 - unflip pairsync, swap cables → QRT bit 1, hel bit 5, pairsync bit 9 → works, cleaner

/- Run 1594 → Flexio lne = Tsettle now → works

/- Run 1596 - LNE = 150μs > Tstable again, hel map (flip 1 → skip 2) Fixed → re analyze backwards
works

- Run 1597 - QRot all - Fixed Tgroup maps ✓ ADC is [illegible]

U

TO DO: a) Update CRL to veto vqwks whenever bad data gets cleared (like inj) with Paul
✓ b) Add vqwk veto to path of vqwk gate signal
c) Update flexio helicity obtaining to be like injector
d) Verify BMW scalers work, move to flexio maybe
e) Send new flexio LNE & SIS3801 LNE to HRSs
↳ Make sure Tsettle & Tstable both present
↳ SIS veto ↳ Hapth LNE

Add veto: added OPORT bit 7 of 8 from TIR as veto in vqwk logic chain
↳ Now event 1 & 2 with qwk data are both empty
↳ Previously 1 was holdover & 2 was empty...
↳ works, needs data-clear improvement as in inj

verify regular scalers: Problem → accidentally sent Tstable as veto instead of Tsettle, fixed now
↳ New Run 1600 CH → works
↳ New Run 1601 All → started messed up HRS scalers... too long, edited LNE on both
↳ Run 1602 → post fix HRS's, still busted & increased fi gate to 500 μs from ~120 μs
↳ Run 1603/4 fix RHRS
↳ Run 1605 → (Fix) LHRS (Broken still) } → Problem is I swapped sending Tsettle previously, now sending Tstable → add logical Tstable in both now
↳ also note that I changed fix to be inside veto now for purity!

To Do:
- Update CRL (a) for qweak clear data
- update flexio helicity decoding (c)
- fix BMW scaler → flexio (d)
- Send new FLEXIO LNE through P.P. (e)
- Verify all signals ok, compaire current setup to prior setup & make perfect map/diagram
- Replace LHRS scaler with spare & verify timings w/ scope
- Add Tsettle LNE for TI standalone mode everywhere (including CH & check injector)

- Run 1606 → swapped P.P. LHRS Tsettle in case I broke LHRS logic module....
→ nope... go check cable
- Run 1607 → try again... said, scaler bad

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Summary of New DAQ

f_2 ✓, f_4 ✓, i7 kenno TTL ✓,

- Made New gates for SIS3801 LNE = 10 μs after Tsettle, 100 ns long, goes to both HRS, LHRS scaler broken... firmware?
- Made new gate for FLEXIO LNE = 150 μs after Tstable, 100 ns long, only goes to CH, HCL decodes, need P.P. for HCL
  ↳ readout needs CRL improvement, HeL - for safety
- Made new gate for VQWK LNE/ext gate = Tstable + 50 ns from gate generator, lasts 800 ns long, vetoed on TIR bit 7 "gates off"
  ↳ veto needs CRL improvement
- Moved all scaler inputs to top Right NIM bin, separated out V2F for BMW + other signals + added new .map to generate folder + labels need to be made
- Cleaned up P.P. Cables to avoid tripping, but now "Tsettle" labels are out-of-date (now I send T stable)