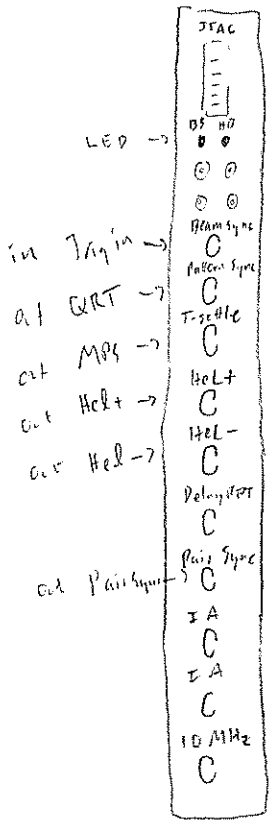
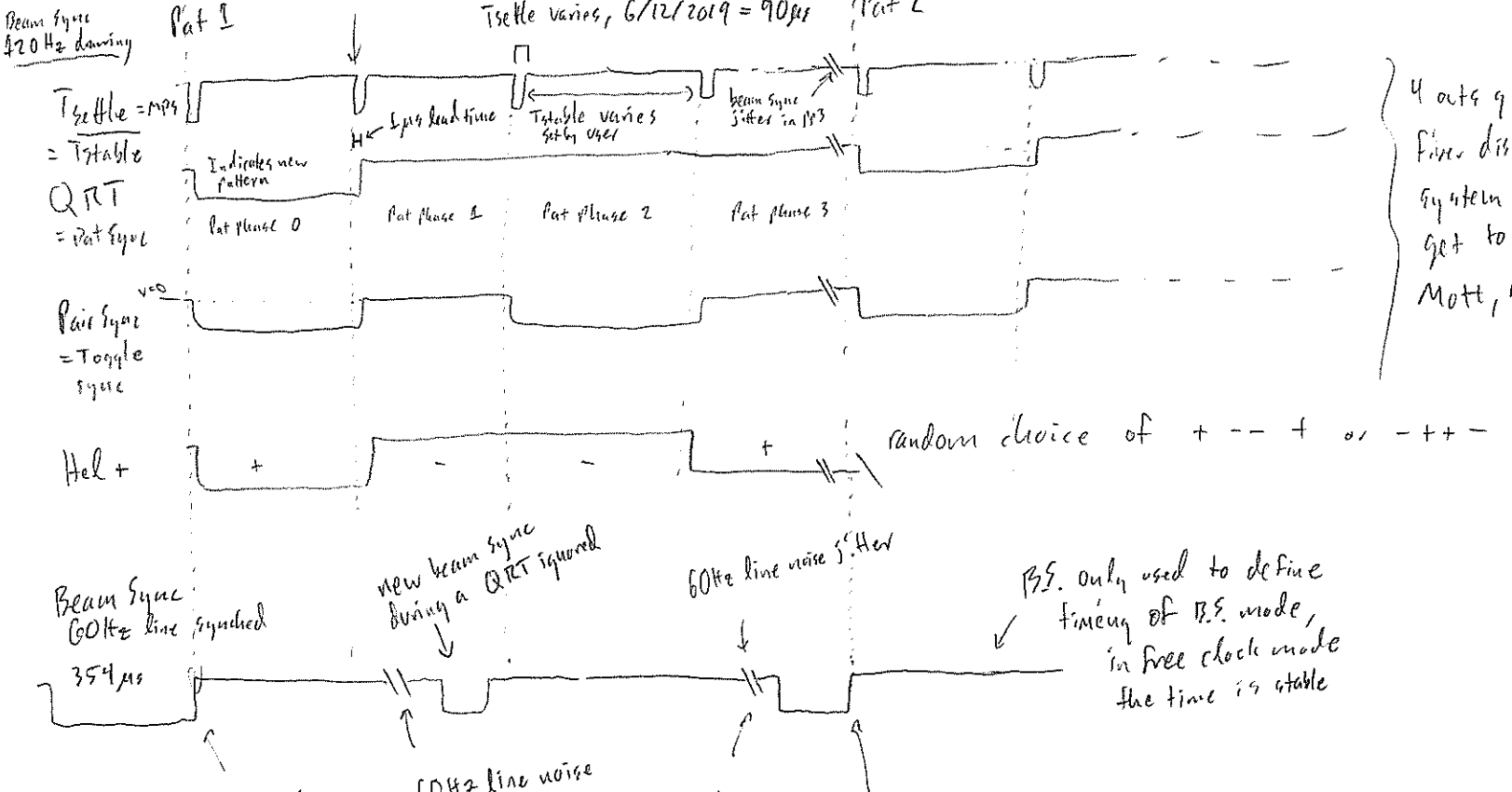
Timing Diagram
Inj Helboard

© Reno
C Fiber

Tstable varies, in Beam Sync mode, Pat Phase 0, 1, 2 Tstable are exactly $(X\,Hz)^{-1}$ − Tsettle
but Pat Phase 3 Tstable last until the next Beam Sync pulse triggers helboard;
IN free clock mode Tstable is exactly the same each time, set by user

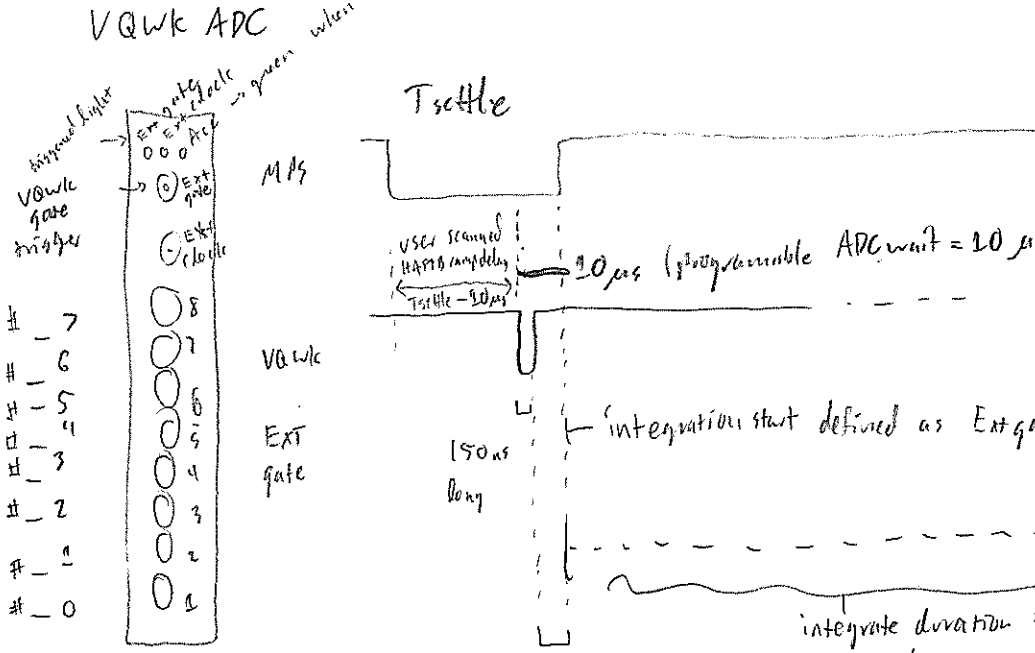
Helicity Control Board





Some Hel JMenu
120, 240, free clock
Tsettle, Tstable
delay number,
Pattern type

VQWk ADC



8333.33μs = (120 Hz)^-1

− 8192μs = 141.33

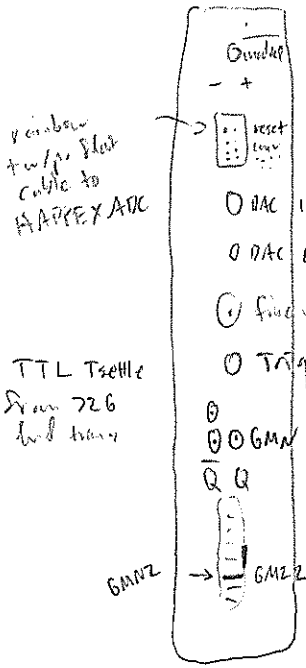
for 90μs Tsettle we get 51.33μs un integrated deadtime (catches Beam sync jitter)

CH input: "VQWk gate" to EXT GATE from CH Lower Left NIM crate slot 5 region 3 out 1-6
region 4 out 3-4

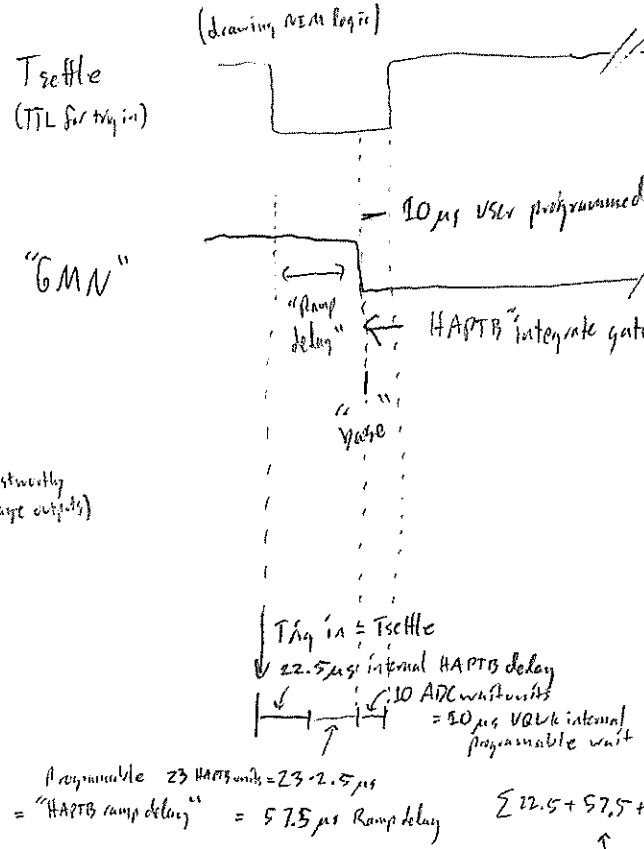
Per VME Module → Drawing of front of module with I/O labelled

Per VME Module → Input & Output timining diagram, and p2p cable map (1 generation)

ex) HAPTB



Timing Diagram (CH, Inj)



CH) P2P Map

= start of HAPTB ramp

Tsettle = TTL lemo cable from 726 in #1, slot 6 ↓ slot

To 726 slot 6, channel #6 ecl (out of GMN2 ecl)

INJ)

GMN2 = start time of ADC gate, cable goes to 726 ecl trans... end is end of SIS 3801 integration

exception) Timing board is different in HRSs, because the SIS & VQWK gates are patched in, so we use HAPTB for old HRS HAPPEX ADC timing

Set HAPPEX ADC integration window == local GMN signal (through rainbow flat cable chain)

This means ramp delay = 10 μs longer (4 more units of TB time → 27 units for 90 μs Tsettle), integration gate time needs to be SIS gate − 4 (−10 μs)

SIS 3801 scaler, slot 5, slot 19

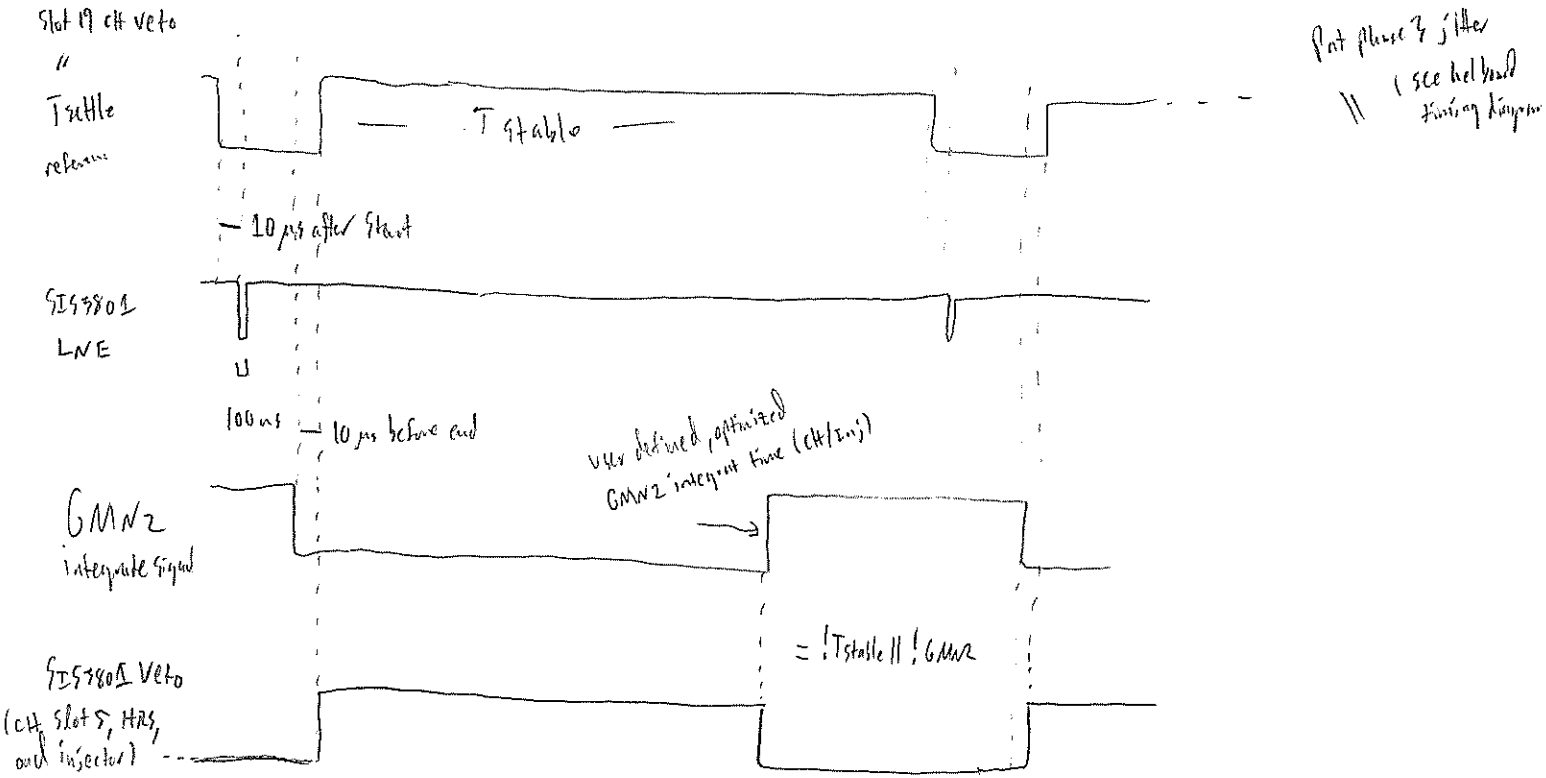
8 control inputs

1 - LNE = 100 ns long pulse 10 μs after tsettle

4 - VETO = !GMN2 || !Tstable for all, but slot 19 CH has Tsettle veto

32 data inputs

↳ integrate # pulses while veto is false



different cables, same timing

SIS3801 scaler slot 5 CH, (Ini, HRSs)

control input 1 (LNE): from CH lower left NIM crate 429A slot 11, region 1, out 3

control input 4 (VETO): $\overline{GMN2}$ || Tsettle from CH lower left NIM crate 429A slot 10, region 4, out 3

3801 scaler slot 19 CH

input 1 (LNE): from CH lower left NIM crate 429A slot 11, region 1, out 4

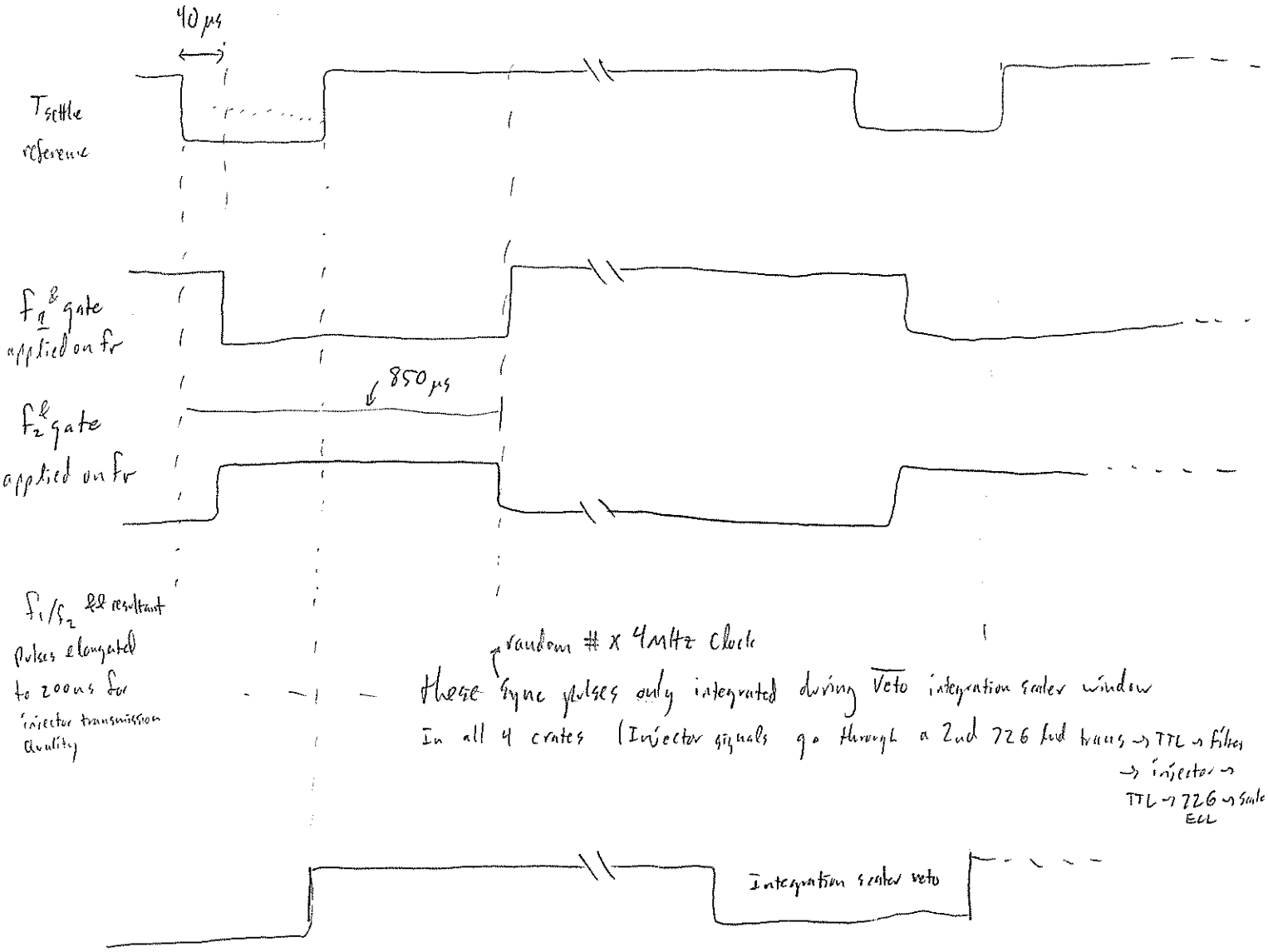
(VETO): from CH lower left NIM crate 757 slot 5, region 3, out 8

(6) Sync Scaler timing Diagram

12 bit DAC from HAPTB → random voltage
↳ V2F ch 16 → translate "f_r"
↳ V2F #1 in Upper Right NIM Bin slot 20 "f_r"
↳ white-black twist to sync, slot 8, 726 upper Right in #1

f_r gets put into gate generators to be gated on off → f_1, f_2

f_r = Constantly "True" series of ~125 ns long pulses

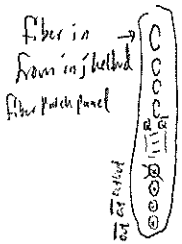


Timing Diagram
CH fiber translators

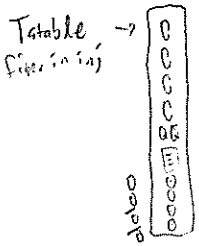
(7)

QRT

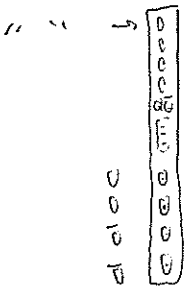
Timing Diagram = Same as helboard



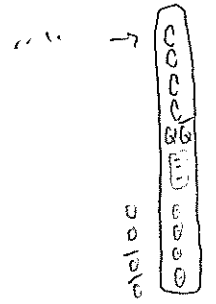
MPS



Hel +



Pair Sync



Outputs

QRT
- ECL 1) empty
- ECL 2) Twisted Pair Differential ECL Pink-grey to FLEXIO-5
- ECL 3) empty
- LEMO 4) Dead
- LEMO 5) empty
- LEMO 6) $\overline{QRT}$ to Moller, P.P. 50ohm to 1H75803, ch #15
- LEMO 7) empty

MPS
- ECL 1,2,3) empty
- LEMO 4) slot 5, 757, input ch# 1, Tstable, for HAPTB trig in (Primary CH)
- LEMO 5) "MPS to Compton", P.P. 50 ohm to 1H75803, ch #18
- LEMO 6) Tsettle to slot 5, 757, input region # 3, Tsettle, for all use
- LEMO 7) Tsettle to ADC CH 5-0 for timing check

Hel
- ECL 1) Tw/pr dECL blue-white to FLEXIO-6
- ECL 2,3) Empty
- LEMO 4) Hel to Moller, P.P. 50Ω to 1H75803 CH #14
- " 5) Hel to underground? Moller?
- " 6) $\overline{Hel}$ "3rd Hel" to Moller probably?
- " 7) $\overline{Hel}$ to compton

Pair Sync
- ECL 1) Twisted pair differential ECL red/black to FLEXIO-7
- " 2,3) Empty
- LEMO 4) "HAPPEX", sends pairsync underground?
- " 5) ?? goes above
- 6) $\overline{pairsync}$ to upper p.p. ch 50Ω to 1H75803 ch #12