1 Parity VAQ CHA NIM Bin lower left

ID	CHA Rack	Type	Module, Slot, Name	Inputs	In type	Timing w/r. Tsettle	Output Destinations	Out Type	Delay (cable...)
a	CH01B03	NIM Bin Helicity Receiver	Helicity Fiber translator, Slot 1, "QRT"	1) Injector QRT from fiber P.P.	Fiber	1 μs after start	1) empty 2) ECL twpr pink-grey to FLEXIO_5	ECL twpr	
							3) empty 4) dead Lemo empty 5) empty		
							6) $\overline{QRT}$ to Moller, ch 15 in CH P.P. 50 Ohm to 1H75B03	LEMO	8 ns
b	" "	" "	Helicity Fiber translator, Slot 2, "MPS"	1) Injector fiber Tstable from P.P.	Fiber	$\overline{Tsettle}$	7) empty 1,2,3) empty	ECL	
						Tstable	4) 757 input ch 1 Tstable	Lemo	1 ns
							5) "MPS to Compton" ch 18 in CH. P.P. 50 Ohm to 1H75B03	Lemo	6 ns
						$\overline{Tstable}$ = Tsettle	6) Tsettle to 757 input region 3	Lemo	1 ns
							7) To CH ADC 5_0 for timing check	Lemo	9 ns
c	" "	" "	Helicity Fiber translator, Slot 3, "Hel"	1) Injector fiber Hel (+?) from P.P.	Fiber	Hel (+?), 1 μs after start	1) blue-white twpr to FLEXIO_6 2,3) empty	Twpr ECL	
						Hel	4) Hel to Moller, ch 14 in CH. P.P. 50 ohm to 1H75B03	Lemo	8 ns
							5) Hel underground, ??? moller?	Lemo	???
						$\overline{Hel}$	6) "3rd Hel" Moller probably ??	Lemo	6 ns
							7) Hel to Compton	Lemo	6 ns
d	" "	" "	Helicity Fiber translator, Slot 4, "Pair Synch"	1) injector fiber Pair Synch from P.P.	Fiber	PairSync, 1 μs after	1) red-black twpr FLEXIO_7 2,3) empty	Twpr	
							4) "Happex" goes underground ???	Lemo/BNC	long ???
							5) ??? goes above	Lemo/BNC	???
						$\overline{Pair\ Sync}$	6) Upper P.P. ch 12 50Ω to 1H75B03	Lemo/BNC	6 ns

CHA NIM Bin lower left

... outs 0 0 0 = 2 3 4 / 0 0 0 = 3 5 6 / 0 0 0 = 4 7 8 — out out

ID	CHA Rack	Type	Module, Slot, Name	Inputs	In Type	Timing w.r.t. Tsettle	Output Destinations	Out type	Delay
e)	CH01B03	NIM Fan in/out	Phillips 757, slot 5 (↳ quad mode FIFO)	Region 1)	lemo	== Tstable = $\overline{Tsettle}$	$\overline{Out}$ 1-4) empty		
							Out 1) FLEXIO LNE trigger, Slot 12 794 g.g. #3	lemo	2 us
							out 2) empty		
							out 3) Upper Right NIM Bin slot 4, 240 input #2	lemo	6 us
							Pick one: out 4) T. Left arm detector stack, P.P. #10	lemo	15 ns (for lemo)
							Pick one: out 5) Moller "3rd MPS" 50 Ohm to 1H75B03 #5	lemo	6 ns (models)
							Pick one: out 6) To Right arm detector stack, P.P. #2	lemo	15 ns
							Pick one: out 7) empty		
							Pick one: out 8) To left arm detector stack, P.P. #6	lemo	6 ns
f)	CH01B03	NIM Fan in/out	Phillips 757, slot 5	Region 2)	lemo	== Tsettle = $\overline{Tstable}$	$\overline{Out}$ 1-4) empty		
							out 1) empty		
							out 2) Raster 1D scope trigger	lemo	15 ns
							out 3) Upper Right NIM Bin, slot 2 726 in ch #5	lemo	8 us
							out 4) Lower Left NIM slot 12 794 in ch 1 trigger (SIS3801 LNE)	lemo	2 us
							out 5) "Moller MPS" P.P. 16 50Ω to 1H75B03	lemo	8 us
							out 6) Upper right NIM bin slot 1, 622 in ch #1 (redundant copies)	lemo	8 us
							out 7) lower NIM Bin slot 6, 726 in ch #1, HAPTB LNE TTL	lemo	1 us
							out 8) VME slot #15 (19th slot), 2nd SIS3801 Veto	lemo	9 us
g)	CH01B03	NIM Fan in/out	Phillips 757, slot 5	Region 3)	lemo	== Vqwk gate (↓ 150 us long pulse; 10 us before Tstable, needs calibration from defined by GMN2 HAPTB)	$\overline{Out}$ 1-4) empty		
							Out 1-6) go to Vqwk EXT gates	lemo	8 us or 50
							out 7) → Region 4 input	lemo	1 us
g cont'd)	CH01B03	NIM Fan in/out	Phillips 757, slot 5	Region 4)	lemo	== Vqwk gate	$\overline{Out}$ 1-4) empty		
							out 1) to RHRS P.P. #8	lemo	15 us
							out 2) to LHRS P.P. #7	lemo	8 us
							out 3, 4) to new 2 vqwk ADCs LNE ext gate	lemo	8 us

3 Parity DAQ CHA NIM Bin lower left

429A def: out 1 2 ; 2 4 ; 5

ID	CHA Rack	Type	Module, Slot, Name	Inputs	In type	Timing w.r.t. Tsettle	output Destinations	out type	Delay
h)	CH01B03	NIM Level trans	Philips 726, 6, level trans	1) = f7 Tsettle	lemo	== Tsettle = $\overline{Tstable}$	TTL) HAPTB trigger	lemo	6us
				2 empty			NIM1) empty		
							NIM2) slot 10, 429A, region 4 in, SIS Veto def	lemo	2us
				3) = Flexio LNE	lemo	== 150 μs after end lasts ~ 200 Ns	ecl) red-blue to FLEXIO LNE tw-pr	red-blue twpr	
				4) = TI out 6 pink-grey Twpr	twpr pink-grey	CRL Timing	lemo/NIM1) To Vqwk veto	lemo	1us
				5) = TI out 7 green-pink Twpr	Twpr green-pink	CRL Timing	No out		
				6) = Hapth GMNZ Grey/Brown Twpr	Twpr grey-Brown	HAPTB timing, 10 μs before Tstable	NIM out 1) Slot 10 429A input region 1 → scaler veto	lemo	1us
				rest empty			NIM out 2) slot 7 755 input region 1 → Vqwk gate	lemo	1us
i)	CH01B03	NIM logic unit	Philips 755, 7, logic	1) GMNZ	lemo	150 us long Pulse at start HAPTB timing, 10 μs before Tstable	out 1) "Vqwk gate" slot 5 775 in region 3 to ADCs LNE's	lemo	3us
j)	CH01B03	NIM G.G.	LeCroy 222, 8, G.G.	→ This is just a home made clock, no use otherwise					
k)	CH01B03	Homemad FR A.C. Switch ... ? → Raster current control?							
l)	CH01B03	Logic FIFO	LeCroy 429A, 10, FIFO	1) GMNZ from h)6)1)	lemo	GMNZ Hapth Timing	out 1) $\overline{GMNZ}$ to self in ch #4	lemo	1us
							out 1) RHRS P.P. # 14 } Scaler VETO	lemo	15us
				4) $\overline{GMNZ}$ self Tsettle from h)1)2)	lemo	== $\overline{GMNZ}$ ∥ $\overline{Tstable}$ Starts on 2nd of Tstable ∥ GMNZ ends first of same	OUT 2) LHRS P.P. # 15	lemo	8us
							out 3) First SIS3801 scaler in VME crate slot 5 VETO		8us
m)	CH01B03	Logic FIFO	LeCroy 429A, 11, FIFO	1) SIS3801 LNE, n)1) delay	lemo	100 us long pulse == SIS3801 LNE = 10 μs after Tsettle	out 1) LHRS P.P. # 9 SIS3801 LNE	lemo	15us
							out 2) RHRS P.P. # 7	lemo	15us
							out 3) first VME SIS3801 LNE, slot 5	lemo	8us
							out 4) 2nd VME SIS3801 LNE, slot 15 (19th slot)	lemo	5us
				3) FLEXIO LNE n)3) delay	lemo	== 150 μs after end Tsettle (or Tstable) lasts ~ 200 ns	out 1) RHRS P.P. # 1	lemo	16us
							out 2) LHRS P.P. # 9	lemo	16us
							out 3) h)1)3, 726 in #3 slot 6	lemo	3us
n)	CH01B03	G.G. delay	Philips 794, 12, G.G.	1) Tsettle from e)2)4	lemo	== Tsettle	Delay) SIS3801 source to Slot 11 in #1	lemo	1us
				3) Tstable from e)1)2	lemo	== Tstable	Delay) FLEXIO LNE source to slot 11 in #3	lemo	1us

4 Pantry VAQ CHA NIM is in Upper Right

ID	CHA Rack	Type	Module, slot, Name	inputs	In type	Timing w.r.t. Tsettle	output Destinations	out type	Delay
0)	CH01B02	Quad Coin	LeCroy 622, slot 1, FIFO	1) Tsettle, b16	Lemo	== Tsettle	2) slot 6 NIM↔ECL NIM in 1)	lemo	6ns
							3) self input 4 → to underground	lemo	12ns
				2) Sync f2 (from slot 3 out 2)	lemo	== Sync f2, 200ns pulses (~850μs after Start)	1) RHRS r.p. #5	lemo	15ns
							2) LHRS r.p. #11	lemo	15ns
							4) slot 2 726 ch #3 input → to CH scaler	lemo	1ns
							5) slot 9 726 ch #2 input → to inj	lemo	4ns
				3) Sync f1	lemo	== sync f1, 200ns pulses (~during Tsettle 40ms)	1) RHRS r.p. #12	lemo	16ns
							3) LHRS r.p. #12	lemo	12ns
							4) slot 2 726 ch #2 input → to ch scaler	lemo	1ns
							5) slot 9 726 ch #1 input → to inj	lemo	3ns
				4) Some crazy signal "to pion + left, Rare Ref unit #2"					to Compton delay . . . ?
1)	CH01B02	Ind trans	Multip 726, slot 2, translator	1) Sync fr, slot 8 ch 8 out	lemo	DAC 12 V2F, CRL Timing	NIM 1) slot 3 756 in #1 to sync f2	lemo	1ns
							NIM 2) slot 3 756 in #2 to sync f1	lemo	1ns
							ECL out) first CH scaler ch_0	flat cable	
				2) Sync f1 0)3)4)	lemo	gated fr = f1	ECL out) first CH scaler ch_1	flat cable	
				3) Sync f2 0)2)4)	lemo	gated fr = f2	ECL out) first CH scaler ch_2	flat cable	
				4) BMW Trig @)3)3)	lemo	BMW Trig-CRL	TTL out) to Bsy trig	lemo-BNC	long
							ECL out) first ch scaler ch_3	flat cable	
				5) Tsettle e)2)3)	lemo	== Tsettle	ECL out) first ch scaler ch_4	flat cable	
							NIM 1) slot 7 794 in #3 f1/f2 marker	lemo	2ns
				6) TI out 0 black-yellow	black-yellow TI out 0	CRL timing	ECL out) first ch scaler ch_5	flat cable	
				8) slot 11 V2F 4MHz	lemo	V2F 4MHz	ECL out) first ch scaler ch_7	flat cable	
				9) Hall C Bcm 1	lemo-BNC	Hall C V2F	ECL out) first ch scaler ch_8	flat cable	
				10) Hall C Bcm 2	lemo-BNC	Hall C V2F	NIM out 2) "Energy unlock" downstairs ...	lemo BNC	downstairs
							ECL out) first ch scaler ch_9	flat cable	
							NIM out 2) " ??? " downstairs ...	lemo BNC	downstairs
				11) Unser	lemo-BNC	V2F unser	ECL out) first ch scaler ch_10	flat cable	
				12, 13, 14, 15	tw/pr	? V2F ?	ABCD signals from below ? → Scaler	flat cable	

out 1-5

5 Vanity VAQ CHA NIM Bin Upper Right

ID	CHA Rack	Type	Module, Slot, name	inputs	in type	Timing wrt. Tsettle	output destinations	out type	delay
Q)	CH01B02	logic unit	Philips 756, 3, gate gen	1) Sync fr	lemo	f_2 output 850ns after tsettle	Out 3) Slot 1 G22 ch # 2	lemo	1 ns
				Veto) slot 7, ch2, gate	lemo				
				2) Sync fr Veto) slot 7, ch2, $\overline{\text{gate}}$	lemo	f_1 output ~40ns inside Tsettle	Out 3) Slot 1 G22 ch # 3	lemo	1 ns
				3) in 1) BMW Flexio in 2) delayed Tsettle from Q)3) delay	lemo lemo	CRL timing + delay	out 3) Slot 2 ch # 4	lemo	2 ns
							out 4) Slot 7 794 in ch # 4, reset	lemo	2 ns
R)	CH01B02	FIFO	Philips 740, 4, FIFO	1) dead end not Q)3) BMW....					
				2) Tstable	lemo	== $\overline{\text{Tsettle}}$	into the depths	lemo-BNC	long
S)	CH01B02	G.G.	Philips 794, 7, G.G	1) Strang delayed compton thing from slot 1 ch 4					
				2) $\overline{\text{Gate of self 3)}}$	lemo	$f_1 + f_2$ generator	gate) f_2 veto signal, slot 3 ch # 1	lemo	2 ns
							$\overline{\text{gate}}$) f_1 veto signal, slot 3 ch # 2	lemo	2 ns
				3) Tsettle, out 5 of slot 2 bul trans	lemo	== Tsettle	$\overline{\text{gate}}$) self 2) input	lemo	2 ns
							delay) BMW trig stuff	lemo	2 ns
				4) BMW Flexio slot 8, out 1 ↳ reset from TI from Q)3) out 4)	lemo	== Flexio timing	$\overline{\text{gate}}$ → nothing ...	lemo	2 ns
							gate → slot 3 in ch 3 &&	lemo	2 ns
T)	CH01B02	dual ECL→NIM translator	translator, 8, dual trans	NIM in 1) Tsettle from slot 2 G22, ch 1	lemo	== Tsettle	ecl out 1) single ended ecl to T5	ecl	
				ecl in 1) Flexio out 1 black-red tw/pr	tw/pr black-red	== CRL timing	NIM out) 5)4) input BMW Flexio	lemo	2 ns
				ecl in 8) ch 16 of slot 10 V2F → DAC 12 V2F	white-black tw/pr	== DAC 12 CRL Timing	Q)4 1 NIM) sync fr → slot 2 726 ch # 1	lemo	3 ns
				NIM in 8) 4MHz from slot 10 V2F	lemo	== 4MHz clock	ecl out 8) to 2nd scaler ch_0	red-black tw/pr	

6 Parity DAQ CH A NIM Bin Upper Right

ID	CH A Rack	Type	Module, Slot, name	Inputs	in type	Timing wrt Tsettle	output destinations	out type	delay
a)	CH01B02	Phillips 726	Phillips 726, 9, bul trans	1) Sync f1, slot 1	lemo	f1 timing	TTL out) ch 1 Tx fiber trans	lemo	6us
				2) Sync f2, slot 1	lemo	f2 timing	TTL out) ch 3 Tx fiber trans	lemo	6us
v)	CH01B02	V2F	V2F, 10, V2F	16) Hapth DAC 12	lemo→V2F	CRL timing	white-black twpr to Sync for slot 8 ecl to Nim in 8	twist	
w)	CH01B02	V2F	V2F, 11, V2F	1 "17" – 16 "32" P.P. from BSY BMW	lemo→V2F	BSY BMW timing	into ch 16 – 31 of first CH scaler	flat cable	
x)	fiber translate	Keith Cole's thing	———	Tx1 = Sync F1	lemo	f1 timing	CH → Inj # 5 fiber	fiber	inj
				Tx3 = Sync F2	lemo	f2 timing	CH → Inj # 6 fiber	fiber	inj

7 Parity DAQ RHRS

Patch Panel #	signal	destination	Time good?
Betty d6	Tstable	NIM bin slot 1, ch2, in 1	yes
Betty d2	SIS3801 LNE	→ Same	yes
Betty d4	Sync f1	→ Scaler in _30	yes
Betty C4	Sync f2	→ Scaler in _31	yes
Betty d5	FLexio LNE	→ Same	yes
Betty C8	SIS3801 Veto	→ Same	yes
Betty d7	VQwk gate	→ NIM Bin Slot 4 726 in #11	yes

429A Slot 1 in # 2 = Tstable

Out # 2 = Tsettle → Slot 4 726 # 5 → TTL → HapTb trig

Out # 1 = Tsettle → Slot 4 726 # 10 → feeds to # 9, nowhere

Out # 3 = Tstable → Slot 4 726 # 16 → nowhere

Vqwk gate → Slot 4 726 in # 11 → Self in # 7
↳ Both NIM outs go to Vqwk ADC LNEs
Out 1 to adc_0, out 2 to adc_1

Sync f1 to Scaler_30, f2 to Scaler_31

Available switch = halla_rightarm-top-sw → ch 1 = RHRS parity VME crate LAN, ↗ chs 17, 19, 21, 23, 24 open
Hatsv 3 port 2 = portserver

LHRS

P.S. upper level → 2 ... to ... ~50 μs VME Crate

Patch Panel #	Signal Upstairs	destination	Time good?	
Betty a11	Tstable	* NIM B 429A FIFO in # 1	yes	
Betty a10	SIS3801 LNE	NIM 726 in # 10	yes	10 μs > Tsettle start ~100 long
Betty a12	FLEXIO LNE	Directly to FLEXIO in	yes	160 μs > Tstable start ~150 long
Betty a13	VQwk LNE	NIM 726 in # 7	yes	10 μs < Tstable start ~160 long
Betty a14	SIS3801 Veto	Directly to scaler veto	yes	! GUWZ !! Tstable
Betty b11	f2 LHRS	* NIM 726 in # 15	yes	
Betty b12	f1 LHRS	* NIM 726 in # 16	yes	

* Tstable FIFO does this:
Makes Out = Tsettle → 726 → TTL out to HAPTB Trig

* The Sync f1 & f2 go into 726 & get ECL output to scaler chs _30, 31

* Green-pink tuler from Hapt6 VME 1 output to TI input_0

VME Crate power to remote controllable

local switch ↘ has this hatsv plugged in, ports 5-7 empty on 164 subnet ↳ harvest for 188

local portserver = hatsv 20